100/101

MP MASTER
MA29027

PRINCETON APPLIED RESEARCH

INSTRUCTION MANUAL

CORRELATION FUNCTION COMPUTERS*

MODELS 100 & 101

PRINCETON APPLIED RESEARCH CORPORATION

PRINCETON, NEW JERSEY

INSTRUCTION MANUAL

CORRELATION FUNCTION COMPUTERS*

MODELS 100 & 101

THIS MANUAL APPLIES SPECIFICALLY TO MODEL SERIAL NO.

Copyright 1967
Princeton Applied Research Corporation
Princeton, New Jersey

All rights reserved. Contents of this publication may not be reproduced in any form without written permission of the copyright owner.

*Patent Pending

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_07406

TO THE ULTIMATE USER OF THIS UNIT

Princeton Applied Research Corporation is interested in seeing that you get maximum benefits from your purchase. We want to send you the latest in maintenance data, helpful suggestions for using the equipment, information on new accessories and the latest advances in the field. Please help us by filling in and returning one of the attached prepaid reply cards. Thank you.

(For subsequent or other users)

I will also be using a PAR

Model #_____, Serial #_____

Name_____, Title_____

Company_____

Address _____

_____

_____

Telephone_____

I plan to use the unit for:_____

I will be responsible for a PAR

Model #_____, Serial #_____

Name_____, Title_____

Company_____

Address _____

_____

_____

Telephone_____

I plan to use the unit for:_____

	Yes	No
Was unit received in good condition?	☐	☐

If not, how can we be of assistance?

First Class
Permit No. 285
Princeton, N. J.

BUSINESS REPLY CARD
No postage stamp necessary if mailed in the United States

Postage will be paid by

PRINCETON APPLIED RESEARCH CORP.

P. .O. BOX 565

PRINCETON, NEW JERSEY 08540

First Class
Permit No. 285
Princeton, N. J.

BUSINESS REPLY CARD
No postage stamp necessary if mailed in the United States

Postage will be paid by

PRINCETON APPLIED RESEARCH CORP.

P. .O. BOX 565

PRINCETON, NEW JERSEY 08540

WHEN YOUR EQUIPMENT REQUIRES SERVICE

(YOUR WARRANTY IS IN EFFECT UNTIL)

A. Contact the factory (609-924-6835) or your local PAR representative to discuss the problem. In many cases it will be possible to expedite servicing by localizing the problem to a particular plug-in circuit board.

B. If it is necessary to send any equipment back to the factory, we need the following information:

1. Model # and serial #.
2. Your name (instrument user).
3. Your address.
4. Address to which instrument should be returned.
5. Your telephone number and extension.
6. Symptoms (in detail, including panel settings).
7. Your purchase order number for repair charges (does not apply to repairs in warranty).
8. Shipping instructions (if you wish to authorize shipment by any method other than normal surface transportation).
9. For your convenience, two service information cards are attached below. Please tape one of these cards or a page proving the above requested information directly to the instrument or equipment being returned.

C. U. S. CUSTOMERS — Ship the equipment being returned to:
Princeton Applied Research Corporation
Route 518 East of Route 206
Princeton, New Jersey

D. CUSTOMERS OUTSIDE OF U.S.A. — To avoid delay in customs clearance of equipment being returned, please contact the factory or the nearest PAR representative for complete shipping information. A list of representatives is included at the rear of this manual.

E. Address correspondence to:
Princeton Applied Research Corp.
P. O. Box 565
Princeton, New Jersey 08540

MY PAR EQUIPMENT REQUIRES SERVICE

It is a Model #_____, Serial #_____
The malfunction is_____

Name_____, Title_____
Company_____
Address _____

Telephone_____, Ext._____
Please return instrument to me at (address)

Via (shipping method)_____
Signed_____
Purchase Order #_____

MY PAR EQUIPMENT REQUIRES SERVICE

It is a Model #_____, Serial #_____
The malfunction is_____

Name_____, Title_____
Company_____
Address _____

Telephone_____, Ext._____
Please return instrument to me at (address)

Via (shipping method)_____
Signed_____
Purchase Order #_____

First Class
Permit No. 285
Princeton, N. J.

BUSINESS REPLY CARD
No postage stamp necessary if mailed in the United States

Postage will be paid by

PRINCETON APPLIED RESEARCH CORP.

P. .O. BOX 565

PRINCETON, NEW JERSEY 08540

First Class
Permit No. 285
Princeton, N. J.

BUSINESS REPLY CARD
No postage stamp necessary if mailed in the United States

Postage will be paid by

PRINCETON APPLIED RESEARCH CORP.

P. .O. BOX 565

PRINCETON, NEW JERSEY 08540

ADDENDA

A.1 NORMALIZING THE CROSS-CORRELATION FUNCTION

INTRODUCTION

In the study of many phenomena such as turbulence structure analysis, it has become standard practice to define a normalized cross-correlation function, the expression for the normalized function being:

$$\alpha_{12}(\tau) = \frac{R_{12}(\tau)}{\sqrt{R_1(0) \cdot R_2(0)}},$$

where $R_1(0)$ is the auto-correlation of R_1 at $\tau = 0$, $R_2(0)$ is the auto-correlation of R_2 at $\tau = 0$, and $R_{12}(\tau)$ is the cross-correlation of R_1 and R_2 at any given value of τ. It can be seen that the value of the normalized correlation coefficient always lies within the interval $(-1 \leqq R_{12}(\tau) \leqq +1)$.

The Model 100 or 101 Correlator can be effectively used to obtain the normalized correlation coefficient. In so doing, however, care must be taken to compute all three of the required functions with the same computation time base (Delay Range in the Model 100, Computation Period in the Model 101). This comes about because the auto-correlation of a function at $\tau = 0$ varies with changes in the computation time base. For example, with a computation time base of 100 microseconds, the value of the function at $\tau = 0$ is the average over the zero-to-one microsecond interval. If the computation time base were increased to 100 ms, the $\tau = 0$ value would then be computed over the zero-to-one millisecond interval. Consequently, it is necessary to determine the normalized coefficient with the computation time base held constant for the three correlations.

PROCEDURE

A suitable technique for obtaining the normalized correlation coefficient using the Model 100 or Model 101 Signal Correlator follows.

(1) Select the computation time base to be used in making the three correlations.

(2) Auto-correlate the two functions separately, taking note of the $\tau = 0$ value in each case. Although the same gain need not be used for both, take careful note of the gain employed, so that when the cross-correlation is performed, the same gain can be applied to the two signals separately as was used in computing their respective auto-correlation functions.

(3) After setting the gain of each channel to the proper value as indicated in the previous step, cross-correlate the two signals.

(4) Calculate the normalization factor by taking the reciprocal of the

square root of the product of the two $\tau = 0$ values obtained in step two.

(5) Calculate the normalized correlation coefficient for any τ value of the function computed in step three by multiplying the voltage at that τ value by the normalization factor calculated in step four.

A.2 EFFECTS OF SAMPLING ON COMPUTED FUNCTIONS

INTRODUCTION

As explained in some detail in the main body of this manual, both the Model 100 and the Model 101 operate by sampling the input waveform, delaying the samples, multiplying the delayed samples by either the original input waveform (auto-correlation) or by a second waveform (cross-correlation), and averaging the lagged products in an RC integrator. Although the general performance of these instruments is excellent, there are limitations in the reproduction of a continuous waveform by a set of discrete samples. If there is significant power in the input at frequencies approaching half the sampling frequency, these components are somewhat modified before being presented to the multiplier, and, as a result, the output of the signal correlator will differ from the mathematical ideal. The sampling process also introduces aliases of the original input; in most cases these may be ignored because the correlation between a signal at one frequency and a signal at a second frequency is zero. One can, of course, construct inputs containing several frequencies which have internal coherence relations arranged such that one frequency will correlate with the alias of another, but the chance of encountering such a signal is remote. If the input signal has significant components at frequencies approaching one half the sampling frequency*, simply increase the sampling frequency by selecting a shorter Delay Range or Computation Period. If the experimenter is working above 100 kHz, this option ceases to be available to him. Consequently, the following discussion detailing the effects of the sampling process on high-frequency input components is provided, with the hope that it will assist him in using the instrument near the upper frequency limit.

The results of the discussion to follow may be simply condensed. In the case of both the auto- and cross-correlation, the effect of the finite sampling frequency is the same as if the true auto- or cross-correlation function were convolved with a boxcar whose width, σ, is one delay channel. The following discussion will show that:

$$C_o(\tau) = \frac{1}{\sigma}\int_o^{\sigma} C_i(\tau+x)dx,$$

where $C_o(\tau)$ is the output of the correlator and $C_i(\tau)$ is the output of an ideal correlator. Throughout the discussion, "$2f_o$" represents the sampling frequency, and the Nyquist frequency is half the sampling frequency or "f_o".

*The sampling frequency is 100/T Hz, where T is either the Delay Range (Model 100) or the Computation Period (Model 101).

DISCUSSION

The notation and methods to be used are those of Tukey and Blackman (The Measurement of Power Spectra, Dover, 1958). We make use of the Fourier transform pair given on page 68: $A(t, \Delta t)$ pairs with $\Delta(f; 1/\Delta t)$, both being infinite sequences, one in the time domain and the other in the frequency domain, of evenly spaced Dirac delta functions, such infinite sequences being referred to as Dirac combs. From page 68:

$$A(t; 1/2f_o) = \sum_{q=-\infty}^{q=+\infty} \delta(t-q/2f_o)$$

and $\nabla(f; 2f_o)$ is the Fourier transform of $A(t; 1/2f_o)$.

Let the input be $G_o(t)$. Then the sampling process can be described as a combination of two operations. The first is the multiplication of the input, $G_o(t)$, by the infinite Dirac comb $A(t; 1/2f_o)$. The output of this operation is:

$$G(t) = G_o(t)\ A(t; 1/2f_o).$$

If $S_o(f)$ is the spectrum of the original input signal, the spectrum of the output of the first operation is the convolution of the spectrum $S_o(f)$ with the transform $\nabla(f; 2f_o)$ of $A(t; 1/2f_o)$, which gives:

$$S(f) = S_o(f) * \nabla(f; 2f_o).$$

Because $\nabla(f; 2f_o)$ is a sum of Dirac delta functions, the result of the frequency domain convolution may be directly written as:

$$S(f) = 2f_o \sum_{q=-\infty}^{q=+\infty} S_o(f-2qf_o).$$

In the region $(-f_o<f<f_o)$ of the spectrum of the output of the first operation, there is added to the original spectrum aliases of input frequencies which originally were outside this band. There is also energy outside the band $(-f_o<f<f_o)$ which comes from the aliasing of frequency components which originally were within this band.

Although these aliasing effects do not in principle distort the auto-correlation that the instrument calculates, frequencies in the input beyond the band passed by the sampling process do use up dynamic range of the instrument, and should be removed, if convenient, before the correlator input.

The spectrum given above for the output of the first operation of the sampling process now needs modification to include the fact that the sampled value is held until the next sampling instant comes along. The holding oper-

ation is a convolution in the time domain of the sequence of data representing delta functions with a boxcar whose length is the intersample interval; the corresponding operation in the frequency domain is multiplication of the spectrum by the Fourier transform of the boxcar. This transform is:

$$Q_o(f) = 1/2f_o \frac{\sin \frac{\pi f}{2f_o}}{\frac{\pi f}{2f_o}} e^{\frac{-i\pi f}{2f_o}}.$$

Including this factor, we finally obtain for the complex frequency spectrum of the sampled waveform:

$$S(f) = \frac{e^{\frac{-i\pi f}{2f_o}} \sin \frac{\pi f}{2f_o}}{\frac{\pi f}{2f_o}} \sum_{q=-\infty}^{q=+\infty} S_o(f-2qf_o).$$

Because the aliases will not contribute to the correlations obtained by the instrument, we may safely put q=0, and find that the essential effect of the sampling process is to filter the signal passing through the "A" channel with a one-channel-wide boxcar. This causes a delay of ½ channel width, and attenuates the higher frequencies in the input by the factor,

$$\sin \frac{\pi f}{2f_o} \Big/ \frac{\pi f}{2f_o}$$

Let A(t) be the input through the A channel, B(t) the input through the B channel, A'(t) the filtered A input, $C_i(\tau)$ the output of the correlator if there were no modification of the signal by the sample and hold process, and $C_o(\tau)$ the actual output of the correlator. Then:

$$A'(t) = \frac{1}{\sigma}\int_o^{\sigma} A(t-x)dx$$

and

$$C_o(\tau) = \frac{1}{RC}\int_{-\infty}^{o} e^{\frac{t}{RC}} A'(t-\tau)\ B(t)dt,$$

where the present is taken as t=0, and the correlation is the function determined by the past history of the inputs A and B. Inserting the expression for A'(t) into the second relation, one obtains (σ=channel width):

$$C_o(\tau) = \frac{1}{RC\sigma}\int_{-\infty}^{o}\int_o^{\sigma} e^{\frac{t}{RC}} B(t)A(t-\tau-x)dxdt.$$

By interchanging the order of integration,

$$C_o(\tau) = \frac{1}{RC\sigma}\int_o^{\sigma}\int_{-\infty}^{o} e^{\frac{t}{RC}} B(t)A(t-\tau-x)dtdx = \frac{1}{\sigma}\int_o^{\sigma} C_i(\tau+x)dx,$$

which is the result desired.

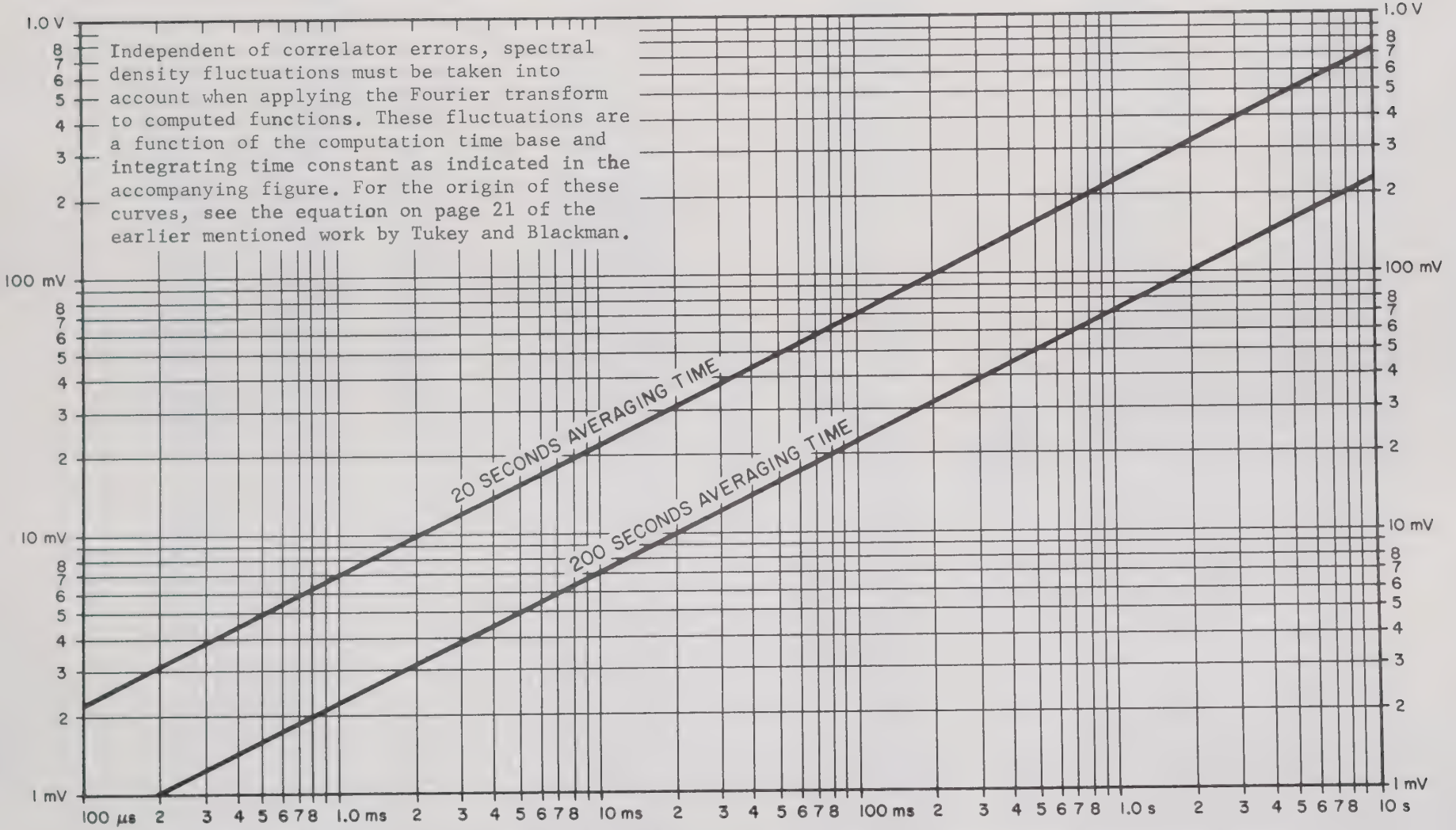
One of the uses to which the Correlator may be put is the determination of the power spectral density. This may be obtained by taking the cosine Fourier transform of the auto-correlation. The convolution operation on the true correlation acts as a filter on the true spectrum to yield an apparent spectrum. The power transfer characteristic of this filter is closely:

$$\frac{\sin\frac{\pi f}{2f_o}}{\frac{\pi f}{2f_o}}$$

The values for which the auto-correlation is available are $\Delta\tau/2$, $3\Delta\tau/2$, etc. In computing the cosine Fourier transform, to maintain phase match at the points where the auto-correlation is available, one should delay by ½ channel width the cosine functions of the delay τ by which one multiples the data points. The formula for evaluation of the power spectrum is:

$$A_k = \sum_{n=o}^{99} C(n)\frac{\cos\pi k(n+\frac{1}{2})}{100}$$

A_k is the amplitude of the power density at the frequency $f_k = k/2T$. The 100 data values of the auto-correlation are labeled by an index "n" running from zero to 99; $\tau = n\Delta\tau$. If side lobes of the spectral analysis window are important, spectra so determined may need modification by hanning, or hamming. This question is discussed extensively in Tukey and Blackman.


Independent of correlator errors, spectral density fluctuations must be taken into account when applying the Fourier transform to computed functions. These fluctuations are a function of the computation time base and integrating time constant as indicated in the accompanying figure. For the origin of these curves, see the equation on page 21 of the earlier mentioned work by Tukey and Blackman.
20 SECONDS AVERAGING TIME
200 SECONDS AVERAGING TIME
1.0 V
100 mV
10 mV
1 mV
100 µs
1.0 ms
10 ms
100 ms
1.0 s
10 s

RMS FLUCTUATIONS IN THE SPECTRAL DENSITY (average value of the estimate, correlator errors not included)

A.3 MANUAL CHANGES AND ADDITIONS

1. Graph on page A-6.

   Observe that this graph plots rms fluctuations in the spectral density as a function of averaging time, with the allowable range of fluctuations being from 1 mV to 1.0 V. It should be clear that this graph is "normalized" to one volt, that is, it is directly applicable only if the rms amplitude of the spectrum is one volt. To be generally applicable, the ordinate values should be changed from their present voltage values to percentage values, the range being from 0.1% to 100%.

2. Output Impedances

   It states throughout the manual that the $C(\tau)$ output impedance is 1 kΩ. This is no longer true, as the impedance has been reduced to 600 Ω. Similarly, the time-base output impedance, indicated in the manual as being 1 kΩ with the slow or medium readout rate has been reduced to 600 Ω, while the fast time-base output impedance is now 11 kΩ "on" and 1 kΩ "off". Because this latter signal is also the Start/Finish Signal supplied to pin F of the rear-panel Interface Connector, the table on page III-25 must be corrected to indicate the new impedance levels.

3. Added Interface Signals

   To operate the Model 100 or Model 101 with the PAR Model 102 Fourier Analyzer, additional interface signals are required. The required wiring is provided in all current production units. The following table lists the four new signals (three outputs and one input) and indicates both the interface connector pin and the board pin at which each signal is available.

INTERFACE CONNECTOR PIN	SIGNAL	ON LEVEL	OFF LEVEL	BOARD AND PIN
M	OA OUT	0 V	+12 V	Counter Board, pin 34
P	11A OUT	0 V	+12 V	Counter Board, pin 35
J	2A OUT	0 V	+12 V	Counter Board, pin 10
E	TRIGGER IN	+3 V	0 V	Counter Board, pin 27

4. Noise

   Figure III-6 (page III-13) shows a family of curves plotting the internal noise of the Correlator as a function of Computation Interval and Averaging Time Constant. Additionally, there exists readout scanning degradation (see MEMORY AND READOUT RESTRICTIONS --- page III-19), which can also be considered a form of "noise". This degradation, in the form of gradual scattering of the stored function with repetitive readout scans, is produced only when the readout scanning circuitry is active and operating at the "FAST" readout rate. Consequently, to prevent this "noise" from adding to the noise indicated in Figure III-6, one need only prevent

fast readout scanning during computation, which is readily accomplished by keeping the Readout Mode Switch set to "SINGLE SWEEP" when computing. After the function is computed, select the readout mode and rate appropriate to the monitoring instrument to observe or record the correlation function.

It should be emphasized that the additional noise (higher than indicated in Figure III-6) produced by computing with the readout circuitry active and scanning at the fast rate, is directly proportional to the Averaging Time Constant. Because, as is indicated in Figure III-6, the internal noise decreases with increasing time constant, the apparent signal degradation produced by allowing fast readout scanning when computing with a long averaging time constant will be far greater than when computing with a short one.

5. Erasure During Computation

If the Readout Mode Switch is set to "ERASE" while the Operation Mode Switch is in either of the two computing positions, erasure will take place in the usual manner. However, if input signals are still being applied, the erasure will not be complete; a small, generally negligible, portion of the arriving information will feed through and be visible at the output. If this signal is objectionable, simply erase with the Operation Mode Switch in the "READOUT ONLY" position. Erasure will then be complete.

TABLE OF CONTENTS

Section			Page
I		CHARACTERISTICS	I-1
	1.1	INTRODUCTION	I-1
	1.2	SPECIFICATIONS	I-2
II		INITIAL CHECKS	II-1
	2.1	INTRODUCTION	II-1
	2.2	PROCEDURE	II-1
III		GENERAL OPERATING INSTRUCTIONS	III-1
	3.1	INTRODUCTION	III-1
	3.2	PRELIMINARY CONSIDERATIONS	III-1
		INSTALLATION	III-1
		POWER REQUIREMENTS	III-2
		FUSING	III-2
		COOLING	III-2
		WARM-UP	III-2
		TEMPERATURE RANGE	III-2
	3.3	OPERATING THE MODEL 100 OR MODEL 101	III-3
	3.4	COMPUTING	III-3
		COUPLING	III-3
		GAIN AND OVERLOAD	III-6
		DELAY RANGE	III-7
		COMPUTATION PERIOD AND PRECOMPUTATION PERIOD	III-9
		NOISE, TIME CONSTANT, AND COMPUTATION INTERVAL	III-12
		OPERATION MODE SWITCH	III-14
		METER SWITCH	III-15
	3.5	READOUT	III-16
		OPERATION MODE SWITCH	III-16
		READOUT RATE	III-16
		READOUT MODE	III-18
		MEMORY AND READOUT RESTRICTIONS	III-19
	3.6	RECORDING	III-19
		STRIP-CHART RECORDERS	III-19
		X-Y RECORDERS	III-20
		OSCILLOSCOPE-CAMERA	III-22
		SMOOTHING	III-23
	3.7	REMOTE PROGRAMMING	III-23
		GATING	III-23
		MEMORY TRANSFER	III-24
		REMOTE TRIGGERING	III-26
		ERASE	III-26
IV		SOME APPLICATIONS OF AUTO- AND CROSS-CORRELATION MEASUREMENTS TO SCIENCE AND ENGINEERING	IV-1
	4.1	INTRODUCTION	IV-1

TABLE OF CONTENTS (Continued)

Section			Page
	4.2	AUTO- AND CROSS-CORRELATION FUNCTIONS	IV-2
V		THEORY AND CIRCUIT DESCRIPTION	V-1
	5.1	INTRODUCTION	V-1
	5.2	INPUT CIRCUITRY	V-2
	5.3	QUANTIZER BOARD	V-3
		PREAMPLIFIER	V-6
		OVERLOAD DETECTOR	V-6
		QUANTIZER	V-7
	5.4	SAMPLER	V-8
	5.5	T-CLOCK	V-8
	5.6	B CHANNEL AMPLIFIER	V-9
	5.7	PRECOMPUTATION DELAY CIRCUITRY (MODEL 101 ONLY)	V-11
	5.8	COMPUTER BOARD CIRCUITRY	V-12
	5.9	OUTPUT BUFFER BOARD	V-14
	5.10	READOUT PROGRAM	V-15
	5.11	TIME BASE GENERATOR	V-20
	5.12	POWER SUPPLIES	V-20
VI		ALIGNMENT PROCEDURE	VI-1
	6.1	INTRODUCTION	VI-1
	6.2	EQUIPMENT NEEDED	VI-1
	6.3	PRELIMINARY STEPS	VI-3
	6.4	POWER SUPPLIES I AND II	VI-3
	6.5	POWER SUPPLY III	VI-4
	6.6	PROGRAMMER	VI-5
	6.7	QUANTIZER	VI-6
	6.8	CHANNEL B AMPLIFIER BOARD	VI-8
	6.9	OUTPUT BUFFER	VI-9
	6.10	INPUT ATTENUATORS	VI-10
	6.11	COMPUTATION INTERVAL CALIBRATION ADJUSTMENT	VI-11
	6.12	ZERO ADJUSTMENTS	VI-12
	6.13	GAIN ADJUSTMENT	VI-14
VII		TROUBLESHOOTING GUIDE	VII-1
	7.1	INTRODUCTION	VII-1
	7.2	WARNING	VII-1
	7.3	SOLDERING TECHNIQUES FOR PRINTED CIRCUIT WORK	VII-2
	7.4	EQUIPMENT NEEDED	VII-4
	7.5	PRELIMINARY STEPS	VII-4
	7.6	POWER SUPPLIES	VII-4
	7.7	ISOLATING THE MALFUNCTION	VII-5
	7.8	COMPUTER SECTION	VII-6
	7.9	OTHER CIRCUITS	VII-8

TABLE OF CONTENTS (Continued)

Section		Page
VIII	WARRANTY	VIII-1
IX	SCHEMATICS (Table of)	IX-1
LIST OF SALES OFFICES		LAST PAGE

FIGURES

Number	Title	Page
II-1	AUTO-CORRELATION FUNCTION OBTAINED WITH SQUARE WAVE INPUT	II-4
III-1	PAR MODEL 100 SIGNAL CORRELATOR	III-5
III-2	CROSS-CORRELATION OF TWO PULSES	III-7
III-3	AUTO-CORRELATION OF WIDE BAND NOISE	III-8
III-4	AUTO-CORRELATION OF BAND LIMITED NOISE	III-9
III-5	CROSS-CORRELATION EXAMPLE TO ILLUSTRATE RESOLUTION IMPROVEMENT CAPABILITIES OF THE MODEL 101	III-11
III-6	TYPICAL BASE LINE NOISE (mV RMS) AS A FUNCTION OF COMPUTATION INTERVAL AND AVERAGING TIME CONSTANT	III-13
III-7	X-Y PLOTS SHOWING EFFECTS OF FREQUENCY RESPONSE MISMATCH	III-22
IV-1	BLOCK DIAGRAM OF AUTO-CORRELATOR	IV-3
IV-2	BLOCK DIAGRAM OF CROSS-CORRELATOR	IV-4
IV-3	CROSS-CORRELATION IN HYDRODYNAMIC TURBULENCE STUDIES	IV-7
IV-4	USING CROSS-CORRELATION TO DETERMINE SYSTEM IMPULSE RESPONSE	IV-8
IV-5	USING CROSS-CORRELATION TO RESPONSE-TEST AN OPERATING SYSTEM	IV-8
V-1	QUANTIZER OUTPUT AS A FUNCTION OF CHANNEL A INPUT AND SAWTOOTH TIME CONSTANT	V-5
V-2	QUANTIZER OUTPUT WITH SINE WAVE INPUT	V-6
V-3	BLOCK DIAGRAM OF CHANNEL B MAIN AMPLIFIER	V-10
V-4	READOUT LOGIC DIAGRAM	V-19
V-5	BLOCK DIAGRAM OF THE POWER SUPPLY SYSTEM	V-21
VI-1	LOCATION OF ADJUSTMENTS AND TEST POINTS	VI-2
VI-2	DISCONTINUITIES FROM IMPROPER ADJUSTMENT OF RAMP LINEARITY	VI-5
VI-3	WAVEFORM PREREQUISITE TO MAKING THE A OVERLOAD ADJUSTMENT	VI-7
VI-4	WAVEFORM OBSERVED WHEN CAPACITANCE OF C_z, C_y, OR C_x, IS TOO LARGE	VI-8
VI-5	WAVEFORM OBSERVED WHEN CAPACITANCE OF C_z, C_y, OR C_x, IS TOO SMALL	VI-8
VI-6	ATTENUATOR TRIMMER CAPACITORS (PANEL LOWERED)	VI-11

TABLE OF CONTENTS (Continued)

FIGURES

Number	Title	Page
VII-1	SOLDER REMOVAL BY WICKING	VII-2
VII-2	TWO SINGLE CHANNEL DISCONTINUITIES	VII-6
VII-3	EFFECT OF FAULTY SHIFT REGISTER STAGE	VII-7

TABLES

Number	Title	Page
III-1	INTERFACE CONNECTOR (J-1) SIGNALS AND LEVELS	III-25
III-2	START/FINISH AND C(τ) OUTPUTS DURING MEMORY TRANSFER	III-26
IV-1	SOME AUTO-CORRELATION FUNCTIONS	IV-5
IV-2	SOME CROSS-CORRELATION FUNCTIONS	IV-6
V-1	READOUT PROGRAM SHOWING COUNTER ADDRESSES	V-17
VI-1	FREQUENCY AS A FUNCTION OF COMPUTATION INTERVAL	VI-12
VII-1	TROUBLESHOOTING VOLTAGES AND WAVEFORMS	VII-9
VII-2	TROUBLESHOOTING VOLTAGES AND WAVEFORMS WHICH APPLY TO MODEL 101 ONLY	VII-10

SECTION I
CHARACTERISTICS

1.1 INTRODUCTION

The PAR™* Model 100 and Model 101 Signal Correlators are designed to compute the auto-correlation or cross-correlation functions of electrical signals varying in time. The cross-correlation function, $C(\tau)$, of two variables is defined by:

$$C_{1,2}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T f_1(t)\cdot f_2(t-\tau)\,dt.$$

For the special case where $f_1(t)$ and $f_2(t)$ are identical signals, $C(\tau)$ may be expressed by:

$$C(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T f(t)\cdot f(t-\tau)\,dt,$$

which represents the auto-correlation function of one variable. Utilizing both analog and digital techniques, these instruments operate as hybrid computers to solve either of the two integrals for one hundred incrementally increasing values of the time delay, $\Delta\tau$. The "n"th point on the correlation function computed is closely represented by:

$$C_n(t) = \frac{1}{RC} \int_{-\infty}^{t} e^{-\frac{t-t'}{RC}}\, v_A(t')\cdot v_B(t'-n\Delta\tau)\,dt',$$

where "RC" is the time constant of the averaging circuits, "$n\Delta\tau$" defines the time coordinate of the computed point, and t' represents the past history of computation, or by definition, $t' > t$.

Computation at each point involves three basic operations, time shifting, multiplication, and integration. The rate of time shifting determines the incremental value of time delay, $\Delta\tau$, and thus sets the time base against which each point of the correlation function is computed. Multiplication of the two input signals is performed automatically at each point. Internal RC networks, the time constant of which determine the averaging time, perform the integration. Because all the mathematical operations involved in evaluating each point are performed simultaneously in real time, the length of time required to compute the complete function depends only on this averaging time constant.

As it is being computed, the correlation function is stored in the 100 channel analog memory. Versatile readout circuitry allows the function to be displayed on an oscilloscope as it is being computed, and to be non-destructively read out either after or during computation. Suitable recording instruments include both strip-chart and X-Y recorders, as well as oscilloscope-camera combinations.

*PAR is a trademark of Princeton Applied Research Corporation.

As with any computer, the computed function is only a good approximation of an ideal result. In the case of the Model 100 and Model 101, conformity of the computed and the ideal function is excellent, their difference typically not exceeding one percent at any point.

1.2 SPECIFICATIONS

GENERAL SPECIFICATIONS (Model 100 and Model 101)

(1) USEFUL FREQUENCY RANGE

DC to approximately 250 kHz.

(2) INPUT VOLTAGE LIMITS

RMS value of the input signal (including DC if DC coupling) should not exceed 200 volts for all ranges of the Gain Switch except the gain-of-five range where the limit is 25 volts. In no case should the instantaneous voltage applied to the input connector exceed ±200 V.

(3) OPERATIONS PERFORMED

Computation of cross-correlation or auto-correlation functions.

(4) OPERATING MODES

(a) COR $0<\tau<T$ (Model 100)
COR (τ) (Model 101) } -- Correlation function computed. Simultaneous readout of the function available.

(b) READOUT ONLY ---------- No computing takes place. Readout capability available.

(c) READ $\tau=0$ ---------- Correlation function computed. Readout of first point only.

(5) OVERLOAD INDICATION

Front panel overload indicator lamps light whenever the dynamic range of the input amplifiers is exceeded.

(6) AVERAGING TIME CONSTANT

Nominally 20 seconds. Can be supplied at any value from 0.1 to 400 seconds. Time Constant can be changed in the field.

(7) MEMORY

The computed function is stored in the memory as 100 discrete voltage levels or pedestals (range of amplitude is 0 ±3.5 volts).

(8) INFORMATION HOLDING TIME

The displacement of any pedestal from its level at the beginning of the hold period will not exceed 30 mV in 10 minutes at 25°C. Read-out scanning restrictions on page III-19.

(9) NOISE AND DYNAMIC RANGE

Output noise is a function of Delay Range (computation period in the case of the Model 101) and Averaging Time Constant. See page III-13 for the family of curves which relate noise to these two factors. Maximum output is ±3.5 V. The smallest signal which can be applied to the input and still yield acceptable results is dependent on output noise, and hence on Delay Range (computation period) and Averaging Time Constant.

(10) COMPUTATION ERROR

Less than 1% of true value.

(11) CALIBRATION

Provision is made for applying an internally derived 1V DC calibrate signal to each channel to obtain 1V of correlated output.

(12) CALIBRATION ACCURACY

±2%.

(13) GATING

Provision is made for inhibiting the computation process on command when correlating low duty factor signals.

SIGNAL CHANNEL CHARACTERISTICS (Model 100 and Model 101)

(1) INPUT COUPLING

DC, AC, GRD., CAL. 1V, and A or B.

(2) INPUT IMPEDANCE (A function of Coupling "Mode" as follows)

(a) DC ---------- 1 M shunted by 50 pF.

(b) AC ---------- 1 M shunted by 50 pF (through 1 μF).

(c) GRD. ---------- Signal input connector disconnected and ground applied to input amplifiers.

(d) CAL. 1V ---------- Signal input connector disconnected and internally derived 1V DC level applied to input amplifiers.

(e) A or B ---------- Input channels cross-coupled for ease in auto-correlation. Input impedance reduced by a factor of two.

(3) GAIN

.01 to 5.0 in 1, 2, 5 sequence.

(4) GAIN STABILITY

Gain variation less than .1%/hour.

(5) ZERO DRIFT

±10 mV/hour.

(6) LINEARITY

Within 1%.

DELAY CHARACTERISTICS (Model 100 only)

(1) DELAY RANGE (total delay duration)

100 microseconds to 10 seconds in 1, 2, 5 sequence.

(2) DELAY (time base τ) ACCURACY

±1% at midrange. ±2% at five fastest and three slowest ranges.

(3) NUMBER OF DELAY INTERVALS

100 (computed simultaneously).

(4) CHANNEL DURATION

One percent of the selected Delay Range. Limits the "resolution" at that value for any Delay Range.

DELAY CHARACTERISTICS (Model 101 only)

(1) DELAY RANGE (Precomputation Period plus Computation Period)

(a) Minimum - 100 microseconds

(b) Maximum - depends on the degree of precomputation capabilities provided with the instrument (as specified by the customer). May be as short as 20 seconds or as long as 100 seconds.

(2) DELAY RANGE ACCURACY

±1% with midrange values of Computation Period. ±2% with five shortest and three longest values of Computation Period.

(3) RANGE OF COMPUTATION PERIOD

100 microseconds to 10 seconds in 1, 2, 5 sequence.

(4) CHANNEL DURATION

1% of selected Computation Period. Limits the resolution to that value for any combination of Computation Period and Precomputation Period.

(5) RANGE OF PRECOMPUTATION PERIOD

In integer sequence, from zero to that multiple of the Computation Period specified by the customer (highest available is nine).

(6) PRECOMPUTATION-COMPUTATION COMPATIBILITY

Satisfactory precomputation operation with all but the shortest (100 microsecond) Computation Period is guaranteed, and though not guaranteed with the shortest Computation Period, it is typically obtainable.

READOUT CHARACTERISTICS (Model 100 and Model 101)

(1) FEATURES

(a) Readout is non-destructive.

(b) Readout can take place either simultaneously with or after computing. The readout rate is independent of the computing rate, even when both occur at the same time.

(2) MODES

(a) CONT. ---------- Automatic and successive readout of the memory contents at any of the provided readout rates.

(b) SINGLE SWEEP ---------- Memory contents scanned once upon triggering.

(c) ERASE ---------- Memory contents reduced to zero in about five seconds.

(3) RATES

(a) FAST ---------- Two points per millisecond - suitable for recording with oscilloscope-camera combination.

(b) MED. ---------- Twelve points per second - best suited to recording with a fast-responding recorder.

(c) SLOW ---------- Two points per second - suited to recording with most strip-chart or X-Y recorders.

(4) PROGRAMMING

Provision for remote control of erase and readout-on-command functions.

(5) SMOOTHING

A rear panel switch allows insertion of a filter which smoothes the output pedestals when reading out at the fast readout rate.

(6) TIME BASE OUTPUTS

(a) Medium and Slow Readout Rates ---------- Positive going zero to five volt staircase (50 mV per step) coincident with the scanning of the memory. Staircase output impedance is 1 k.

(b) Fast Readout Rate ------ Positive going plus one to plus twelve volt pulse coincident with scanning of the memory. Output impedance is 20 k.

OTHER CHARACTERISTICS (Model 100 and Model 101)

(1) MONITOR

Front panel meter and associated switch allow monitoring of memory contents or time base output. Time base output level gives indication of which memory element is being monitored.

(2) POWER REQUIREMENTS

105-125 V AC or 210-250 V AC, 50-60 Hz, 135 volt amperes.

(3) SIZE

19" W x 20 5/8" D x 8" H.

(4) WEIGHT

50 pounds (shipping weight = 62 pounds).

(5) MOUNTING

Rack or bench.

SECTION II
INITIAL CHECKS

2.1 INTRODUCTION

The following paragraphs are provided to facilitate initial performance checking of either model PAR Signal Correlator. In general, the following procedure should be performed after inspecting the instrument for shipping damage (any noted to be reported to the carrier and to PAR) but before using it experimentally. As the procedure presupposes no knowledge of the instrument on the part of the checker and requires little equipment, it can easily be performed by personnel not directly involved with experimental use of the Correlator. The check-out procedure should be performed in the indicated sequence if proper results are to be obtained. Should any difficulty be encountered in carrying out these checks, remove the top cover of the instrument (the top cover is held by two screws on the underside of the rear edge) and ascertain that all circuit boards are securely seated in their sockets. If after so doing the problem persists, contact the factory or one of PAR's authorized representatives, a list of whom appears at the end of the manual.

2.2 PROCEDURE

(1) Using the linecord provided, connect the correlator to a 115V, 60 Hz power line. EXCEPTION: Export models bearing red tags attached to the plug end of the power cord should be connected to the power source indicated on the tag.

(2) Turn the front panel Power Switch on. Note that the fan (located at the rear of the instrument) is operating and that the panel meter lamp lights.

(3) Allow the instrument to warm up for no less than one half hour.

(4) Set the front panel controls as follows.

(a) Model 100 and Model 101

A channel GAIN	.5
A Channel COUPLING	GRD.
METER SWITCH	$1V^2$
B Channel GAIN	1
B Channel COUPLING	CAL. 1V
READOUT RATE	SLOW
READOUT MODE	ERASE for ten seconds, then switch to CONT.

(b) Model 100 only

SIGNAL A DELAY RANGE T	.2 mSEC.
OPERATION MODE	COR. $0<\tau<T$

(c) Model 101 only

COMPUTATION PERIOD T ---------- .2 mSEC.
PRECOMPUTATION PERIOD ---------- fully clockwise
OPERATION MODE ---------- COR (τ)

(5) Observe the following.

(a) The panel meter should indicate approximately zero (center scale) and should stay within five divisions of its initial indication for five minutes.

(b) Both Overload Lamps should be off.

(c) The Ready Lamp should flash briefly once a minute.

(6) Set the front panel controls as follows (Model 100 and Model 101).

A Channel GAIN ---------- 5
A Channel COUPLING ---------- CAL. 1V
METER SWITCH ---------- TIME BASE
B Channel GAIN ---------- 5
READOUT RATE ---------- MED.
READOUT MODE ---------- SINGLE SWEEP

(7) Observe the following.

(a) Both Overload Lights should be on and the Ready Light should come on within 12 seconds.

(b) The panel meter should indicate zero plus or minus two divisions.

(c) When the TRIGGER button is pressed, the "READY" light should go out and the meter indication should increase smoothly to full scale in about ten seconds. Then the meter indication will rapidly return to zero as the "READY" light comes on again.

(8) The following steps check the overall operation by computing the autocorrelation function of a square wave. The following additional equipment is required.

(a) A general purpose calibrated oscilloscope such as the TEKTRONIX 502 or 543 with a type CA plug-in.

(b) A 1 kHz, two volts peak-to-peak square wave source, if such a source is not provided by the oscilloscope.

(c) Cables appropriate for connecting the above to the Correlator.

(9) Set the front panel controls as follows.

Step 9 continued.

(a) Model 100 and Model 101

A Channel GAIN	1
A Channel COUPLING	AC
METER SWITCH	OFF
B Channel GAIN	1
B Channel COUPLING	A
READOUT RATE	FAST
READOUT MODE	ERASE
SMOOTHING (rear panel)	ON

(b) Model 100 only

SIGNAL A DELAY RANGE T	2 mSEC.

(c) Model 101 only

COMPUTATION PERIOD T	2 mSEC.
PRECOMPUTATION PERIOD	T

(10) Connect the oscilloscope to the Correlator as follows.

(a) Oscilloscope vertical input to the Correlator $C(\tau)$ BNC connector.

(b) Oscilloscope trigger input to the Correlator TIME BASE BNC connector.

(11) Set the oscilloscope controls as follows.

Vertical Sensitivity	0.5 V/cm
Vertical Coupling	DC
Sweep Rate	5 ms/cm
Triggering	External, DC, "+" Slope
Triggering Level or Threshold	Somewhat positive, adjust for good triggering.

(12) Apply the 1 kHz, two volts peak-to-peak square wave to the A INPUT of the Correlator.

(13) Set the READOUT MODE Switch to CONT.

(14) Observe that the oscilloscope now begins to display a triangular waveform like the letter "W". The waveform should be 50 ms wide (10 cm) and should gradually grow to an amplitude of two volts peak-to-peak (4 cm), as shown in Figure II-1. NOTE: AMPLITUDE, FREQUENCY, AND SYMMETRY INACCURACIES IN THE INPUT WAVEFORM WILL CAUSE THE OBSERVED WAVEFORM TO DIFFER SOMEWHAT FROM THAT SHOWN IN FIGURE II-1.

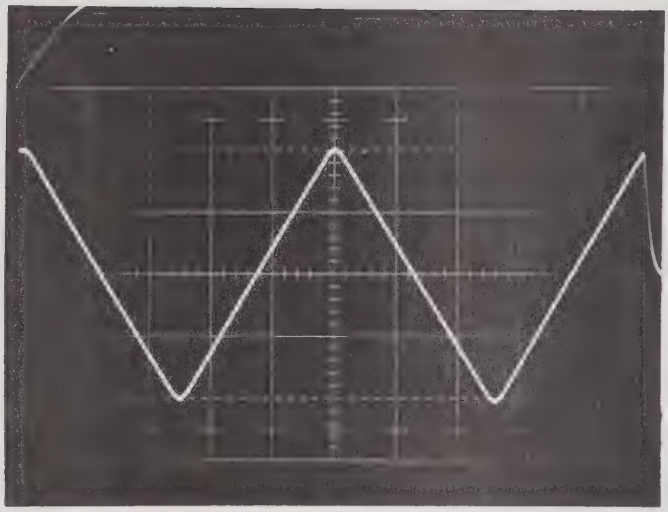


Figure II-1. AUTO-CORRELATION FUNCTION
OBTAINED WITH SQUARE WAVE INPUT

This completes the initial checks. If the instrument performed as indicated, one can be reasonably sure that no malfunctions exist. In general it is neither necessary nor advisable to carry out the alignment procedure (Section VI of the Manual) upon receipt of a new instrument.

SECTION III
GENERAL OPERATING INSTRUCTIONS

3.1 INTRODUCTION

Although the Model 100 and Model 101 are basically simple instruments to operate, some care must be taken if maximum performance is to be achieved. Consequently, the following pages dealing with their operation are provided. Beginning with such preliminary considerations as installation, cooling, and power requirements, their operation is treated in detail. Except where otherwise indicated, the operating instructions apply to both models.

There are many references throughout the operating instructions to the "COR. $0<\tau<T$" position of the Operation Mode Switch. In the case of the Model 101, the front panel symbolization corresponding to this position of the Operation Mode Switch is "COR (τ)." Despite the different symbolization, the two are identical. If the unit in use is a Model 101 Signal Correlator, one has only to be aware that all references to "COR. $0<\tau<T$," are in fact, references to "COR (τ)."

3.2 PRELIMINARY CONSIDERATIONS

INSTALLATION

PAR Signal Correlators can be either bench or rack mounted, and if rack mounted, can be equipped with "slides" to facilitate moving the instrument in and out of the rack. Suitable slides can be purchased from:

JONATHAN MANUFACTURING COMPANY
1258 TEANECK ROAD
TEANECK, NEW JERSEY

To slide-mount the instrument, the following parts, or their equivalents, will be required.

QUANTITY	ITEM
1 pair	STEEL BALL BEARING SLIDE, QUICK DISCONNECT, PART NUMBER 110 QD-16-1 or 110 QD-18-1 (the "16" and "18" refer to the length of the slide in inches)
4	MOUNTING BRACKET, PART NUMBER SP-0440

Mounting the slides necessitates removal of the Correlator side panels, which slide free after the top and bottom covers are removed. The top cover is held in place by two screws on the underside of the rear edge. The bottom cover is held in place by the two screws which hold the two rear rubber feet in place.

If the unit is rack mounted without slides, some sort of support should be provided at the rear.

POWER REQUIREMENTS

Approximately 135 volt-amperes at either 105-125 V or 210-250 V, 50-60 Hz, are required. Changeover from one operating voltage to the other is accomplished by operating a rear panel slide switch. Because this switch is normally covered by the "lip" of the bottom cover, the cover must be removed prior to making a changeover. For operation from 105-125 V, "115" should show in the switch "window," and for operation from 210-250 V, "230" should show.

FUSING

There are seven fuses in all, one line fuse, located on the rear panel, and six internal power supply protection fuses, two of which are located on each of the Power Supply Boards. The line fuse is a slow-blow type rated at two amperes and 250 V. The four fuses located on Power Supply Boards One and Two are fast-blow fuses rated at 1/2 ampere. Of the two fuses located on Power Supply Board Number Three, one is rated at 3/4 ampere, and the other at three amperes. Both are of the fast-blow type. Figure VI-1, page VI-2 indicates the location of these fuses.

COOLING

PAR Correlators use forced-air cooling by an internal fan. As the covers play an important role in channeling the air flow, the instrument must be operated with the covers in place to prevent excessive temperature rise. Before placing an instrument in operation, ascertain that the two rear panel ventilation ports are unobstructed. Also, if the unit is mounted in a cabinet, be sure to allow new air to circulate freely through the cabinet.

A removable filter in front of the fan prevents dust build-up. Because the filter depends on a light coating of oil to trap the dust particles, it will be necessary from time to time to spray the filter with the filter coating oil available from the ROTRON Corporation. Eventually, dust build-up on the filter may significantly impede the air flow and the filter will have to be washed. Ordinary tap water and detergent are suitable.

In addition to the electrical overload protection provided by the fuses, thermal overload protection is provided by a thermostat which interrupts line power when the internal temperature exceeds 66°C. Some factors which could cause the thermostat to "cut out" are obstructed ventilation ports, an excessively dirty filter, or prolonged operation with the covers off.

WARM-UP

A warm-up period of no less than one hour is advised to allow the circuits to reach thermal equilibrium. With lesser warm-up periods, output offsets may degrade the data obtained.

TEMPERATURE RANGE

The instrument can be operated over an environmental temperature range of 15°C to 45°C.

3.3 OPERATING THE MODEL 100 or MODEL 101

Following the one-hour warm-up period, the operator may proceed to compute and record the correlation function(s) resulting from his experiment. Because computing the function and recording it are independent operations, they will be considered separately. As a convenience in following the many references to the front panel controls, Figure III-1, a photograph of the Model 100, is provided on page III-4.

3.4 COMPUTING

Observing the instrument, note the Operation Mode Switch, with which any one of the three operating modes may be selected. Computation of the correlation function takes place when the switch is set to either "COR. $0<\tau<T$" or to "READ $\tau=0$". Once the Operation Mode Switch is in one of these two positions, cross- or auto-correlation can be performed. In the third position, "READOUT ONLY", computing is stopped, although a function already computed and stored can be recorded.

COUPLING

There are two identical Coupling Switches, one for each of the input channels. Each of the switches has five positions, of which two, "DC" and "AC", are true coupling positions, that is, positions in which a signal connected to the associated BNC connector is routed to the input amplifier of that channel. The remaining three positions are special coupling modes; in "GRD." and "CAL. 1 V" the input signal is disconnected from the correlator altogether, and in "A" and "B" (whether "A" or "B" depending on which Coupling Switch is being considered) the input amplifier of that channel is connected to the Coupling Switch of the other channel to facilitate auto-correlation operation. Considering the function of the five coupling modes more closely:

(1) DC COUPLING

With "DC" selected, both the DC and AC components of the input signal will be applied to the input amplifiers. The input resistance is one megohm shunted by 50 pF. Except in those cases where AC coupling allows greater dynamic range (such as when the input signal is a zero referenced square wave or contains a large DC component), it is advantageous to use DC coupling because the low frequency components of the input signal will be coupled to the correlator without phase-shift or attenuation.

(2) AC COUPLING

If the signal has a DC component which is large or of no interest, it may be advisable to use AC coupling, the advantage being that by blocking the DC, the full dynamic range of the input amplifiers will be available to the signal of interest. The disadvantage of AC coupling is that the coupling capacitance, together with the input resistance, forms a high pass filter, the three dB down point of which is 0.16 Hz. Should the signal contain both an undesirable DC component and frequency components which are too low for the AC coupling

Figure III-1. PAR MODEL 100 SIGNAL CORRELATOR

PAR MODEL 101 SIGNAL CORRELATOR

network, simply form a new coupling network with a lower rolloff frequency by coupling the input signal through an external capacitor with the Coupling Switch in the DC position. The value of the capacitor should be 0.16/f microfarads, where "f" is the desired three dB down frequency in Hz.

(3) GRD. and CAL 1V

When the Coupling Switch is in the "GRD" position, the input BNC connector is disconnected from the correlator circuitry and ground is applied to the input amplifier. With the switch in the "CAL. 1V" position, the Input Jack remains disconnected, but the internally derived one volt DC calibrate level is applied to the input amplifier to facilitate gain calibration. A procedure for checking and, if necessary, adjusting the gain calibration is provided below. Realize however, that all instruments are calibrated before leaving the factory, and there should be no need to routinely check the gain.

(a) Select "CAL. 1V" with both Coupling Switches.

(b) Set both Gain Switches to "1".

(c) Set the Meter Switch to "$1V^2$".

(d) Select "COR. $0<\tau<T$" with the Operation Mode Switch.

(e) Set the Readout Rate and Readout Mode Switches to "FAST" and "CONT." respectively.

(f) Model 100 - Set the Delay Range Switch to 10 milliseconds.

Model 101 - Set the Precomputation Period and Computation Period Switches to "0" and "10 mSEC." respectively.

(g) After allowing the panel meter indication to reach its final value (units are shipped with a 20 second time constant unless the customer specifies otherwise), adjust the Rear Panel "GAIN" Control for exactly full scale indication.

(4) A or B

The fifth position of the Coupling Switch provides coupling of both channels to the same input connector for auto-correlation. For example, to perform auto-correlation of a signal applied to the A Channel input, the B Channel Coupling Switch should be set to "A". Likewise, the B channel signal may be auto-correlated by setting the A Channel Coupling Switch to "B". The fact that both input amplifiers are connected to the same input connector in no way interferes with the choice of "AC" or "DC" coupling, or for that matter, "GRD." or "CAL. 1V" coupling, the only difference being that the input resistance is decreased from one megohm to 500 kilohms, with a subsequent rise in the three dB down AC coupling frequency from 0.16 Hz to 0.32 Hz. Realize, however, that <u>both</u> Gain Switches remain effective and are normally set to the same gain.

GAIN AND OVERLOAD

Two factors, the first being the general desire to achieve the highest possible signal-to-noise ratio at the output, and the second being to operate below the level which produces overload of the input channels, determine the optimum setting of the Gain Controls during any given experiment.

Because noise applied to the input of the Correlator only contributes to the output correlation function if there is correlation between the noise and the signal with which it is being compared, output noise is noise arising in the Correlator circuitry. As this noise is independent of gain, it will constitute the smallest fraction of the computed function and so cause the least degradation to it when the gain is as large as possible. The maximum allowable gain, however, is determined by the overload limit of the input amplifiers. The signal just at the overload threshold is 2/G volts, where G is the gain setting of either channel.

In some applications it may be necessary to use long delay times (Computation Period in Model 101) while performing correlations of wide band noise. Because long delay times result in slow sampling rates, the instrument will not be able to handle the higher frequency components of the noise. By passing the signal through a suitable low pass filter before application to the correlator, the bandwidth of the noise is lowered. As a result, higher gain without overload is achieved and a higher amplitude correlation function obtained. A single section RC low-pass filter with a time constant of 16×10^{-4} T ("T" being the setting of the Delay Range or Computation Period Switch) will generally suffice.

To determine the optimum setting of either Gain Control, increase the gain until overload occurs as indicated by the Overload Light. Then "back off" one step. This general rule does not necessarily apply if the input signals are noisy, as long as the average noise amplitude is below the overload level. If the Overload Light comes on occasionally, indicating a clipped pulse of noise, leave the setting of the Gain Control as is, because the net contribution of such occasional overloads to the correlation function will be negligible.

It may occur that the amplitude of an input signal is much too small to achieve the desired "slightly less than overload" condition in the input channels, with resulting noise degrading of the output function. In such cases, preamplify the input signal to raise it to the necessary level.

The setting of the Gain Controls is not the only factor which determines the amplitude of the output function; there must be correlation between the signals being compared to obtain an output. If both signals are DC, the output will be a DC level proportional to both the magnitude of the input DC levels and the setting of the Gain Controls. For signals varying in time, the instantaneous amplitude of the correlation function, expressed in terms of the gain settings of both channels and the instantaneous value of the input signals is:

$$C(\tau) = \lim_{T\to\infty} \frac{G_A \cdot G_B}{T} \int_0^T v_A(t) \cdot v_B(t-\tau)\, dt,$$

where "G_A" and "G_B" are the gain settings, "v_A" and "v_B" are the input signals, and "T" is the averaging time.

DELAY RANGE

In the PAR Model 100 Signal Correlator, the interval over which a correlation function is computed comprises 100 $\Delta\tau$ increments, each having a duration of T/100, where "T" is the Delay Range selected with the front panel "SIGNAL A DELAY RANGE T" Switch. Because the function is always computed over the selected Delay Range, and moreover, always consists of 100 pedestals, each having a duration of one percent of the Delay Range, the delay range setting directly determines the resolution. Besides determining resolution and the correlation time base, the delay range setting, together with the averaging time constant of the instrument, determines the amount of noise which appears at the output.

Frequently it may be advantageous to compute the function at several different Delay Ranges, though as a general rule, one should choose a Delay Range which is long enough to include the interval over which one wishes to correlate, but not so long as to cause undue loss of resolution. Consider briefly how this general objective relates separately to auto- and cross-correlation.

Assume a hypothetical cross-correlation experiment. Some physical event is giving rise to a signal, and at some later time a second signal is detected at another location. The object of the experiment is to determine the degree of correlation between the two signals. Because the second signal arises later than the first, the first must be delayed if the two are to be correlated. As the Delay Range Switch affects the A Channel only, the desired delay can be inserted if the first signal is applied to Channel A. So long as the selected Delay Range includes the interval between the two signals, the correlation function can be computed. Figure III-2 shows the cross-correlation of two pulses.

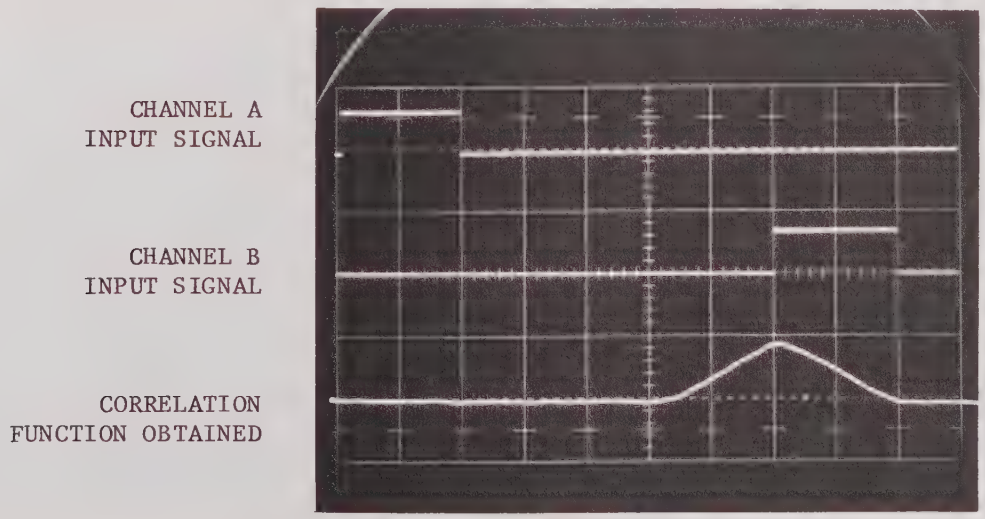


Figure III-2. CROSS-CORRELATION OF TWO PULSES

When auto-correlating, the input signal is compared with itself and the computed function always has its greatest value at τ equal zero. With increasing τ, the coherency of the signal with itself decreases and the amplitude of the obtained function becomes smaller until, with a sufficiently long τ, the function disappears into the baseline noise. The Delay Range which allows any given auto-correlation function to be best displayed depends on the randomness of the input signal. With an input of wide band noise (Figure III-3) the rate of decay is very fast and a short Delay Range is called for. With less random input signals, the correlation function decays more slowly. It may decay relatively smoothly (the spectrum is not centered about one frequency) or ring down (the spectrum is centered about one frequency, as illustrated in Figure III-4). In any case, with less random input signals a longer Delay Range is required.

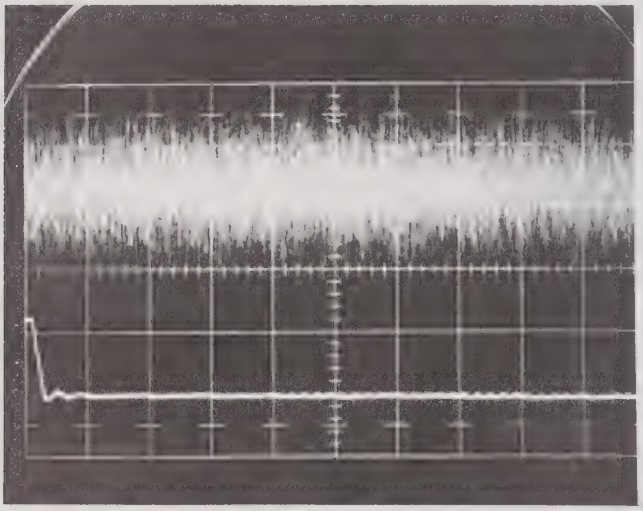


Figure III-3. AUTO-CORRELATION OF WIDE BAND NOISE

To quantitatively express the frequency response or "resolution" of the Model 100 is difficult, both because the instrument utilizes a random sampling technique and because the computed function is stored as 100 discrete pedestals. If the highest frequency component of the correlation function does not exceed 10/T Hz, where "T" is the selected Delay Range, no less than 10 pedestals will constitute one cycle of the highest frequency component, and the distortion of this component will not exceed a few percent. For those frequency components which are lower and consequently are represented by a greater number of pedestals, the distortion is even less. In addition, the effects of the sampling technique must be considered. When the fundamental frequency of an input signal is very near the sampling frequency, beat patterns arise which may obscure the correlation function. Similarly, if one of the harmonics of the input signal is exceptionally large, beats between the harmonic and the sampling frequency may be troublesome. Inasmuch as the sampling frequency is 100/T Hz, where "T" is the selected Delay Range, it is apparent that beat pat-

terns become a problem only when one is pushing the frequency response of the instrument to the limit. If beat patterns do arise, simply choose a longer Delay Time.

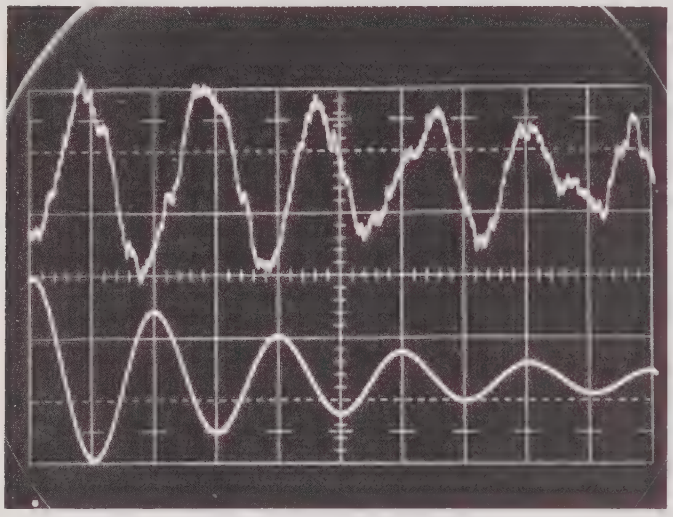


Figure III-4. AUTO-CORRELATION OF BAND LIMITED NOISE

COMPUTATION PERIOD AND PRECOMPUTATION PERIOD

The Model 101 is essentially the same as the Model 100, the significant difference being that in the case of the Model 101, provision is made for dividing the Delay Range into two portions, a Precomputation Period and a Computation Period. As a result, the Channel A Signal can be delayed by the selected Precomputation Period before the Computation Period begins. The Computation Period in turn corresponds exactly to Delay Range in the Model 100, that is, the correlation function is computed as 100 consecutive pedestals, each having a duration of 1% of the Computation Period. By choosing appropriately the combination of Precomputation Period and Computation Period, a given function can be computed with greater resolution than would be the case with the Model 100.

Two front panel controls allow the operator to choose the required combination. The first of these is the "COMPUTATION PERIOD T" Switch, which like the Delay Range Control in the case of the Model 100, allows one to choose computation time base ranges from 100 microseconds to 10 seconds. Immediately to the right of this control is the "PRECOMPUTATION PERIOD" Switch, with which the desired Precompuation Period is selected in multiples of the Computation Period. The range of Precomputation Period available is that specified by the customer. In a unit equipped with minimum precomputation capabilities, the switch has two positions, "0", in which position the instrument is exactly equivalent to the Model 100, and "T", in which position a precomputation delay equivalent to the selected Computation Period is inserted. Units with greater precomputation capability have more positions, allowing one to select "2T", "3T", and so forth,

up to the maximum available of "9T." The precomputation range of an instrument with less than "9T capabilities" can be expanded at any time by installing additional shift register modules, which can be obtained from PAR, and then changing the stop setting of the Precomputation Period Switch. Sockets for installing the additional shift registers are already installed on the Digital Delay Line Board.

Figure III-5 shows how a given correlation function can be examined in detail by making use of the precomputation capabilities of the Model 101 Signal Correlator. First consider Figure III-5(a) which shows a cross-correlation function computed with the Model 100. Note that the duration of the function is ten milliseconds, that is, it "fits" exactly into the selected Delay Range of ten milliseconds. A close examination of the function shows some "detail" at points "a", "b", "c" and "d." Consider how one might proceed to examine this detail more closely. One method might be to appropriately set the recorder controls to "expand" the detailed portion of the function. However, the 100 point resolution limit of the correlator would prevent any significantly increased information recovery by this method. If one were primarily interested in the detail at point "b", the function could be recomputed with a shorter delay range (5 ms) as shown in Figure III-5(b). Relative to Figure III-5(a), the resolution is improved by a factor of two. No further improvement in the resolving of the detail at point "b" can be accomplished with the Model 100; the next shortest delay range, 2 ms, would put point "b" off-scale. In addition, if one were interested in points "c" and "d", no improvement at all over Figure III-5(a) could be obtained with the Model 100. Points closer to the beginning of the function, such as point "a", could be expanded with improved resolution by choosing shorter values of Delay Range, the limit being when the delay range selected is too short to "bracket" the point or interval of interest.

Now suppose the same function were computed with a Model 101 Correlator. Figure III-5(a) would result from a Precomputation Period of "0" and a Computation Period of ten milliseconds. To produce the function illustrated in Figure III-5(b), the Computation Period would be reduced to five milliseconds and the Precomputation Period maintained at "0." It would have been impossible to expand at all the second half of the Figure III-5(a) function with a Model 100 Correlator. With a Model 101 Correlator however, the second half of the function could be expanded. This expanded function, which allows closer examination of the detail at points "c" and "d", is shown in Figure III-5(c). It is produced by using a Computation Period of five milliseconds and a Precomputation Period of "T." Recall that the maximum resolution improvement for examining point "b" with the Model 100 is a factor of two. A much greater resolution could be obtained with the Model 101. By observing Figure III-5(a), it is apparent that point "b" is located a bit more than four milliseconds from the beginning of the function, suggesting that a Precomputation Period of four milliseconds would be appropriate for expanding the detail at point "b." Because the Precomputation Period is in multiples of the Computation Period, it is necessary to select a Computation Period of one millisecond to obtain the desired delay. Figure III-5(d) illustrates the function computed with the indicated combination, that is, with the Precomputation Period Switch set to "4T" and the Computation Period Switch set to "1 mSEC." Relative to Figure III-5(a), the resolution is improved by a factor of ten. Similarly, one could expand any por-

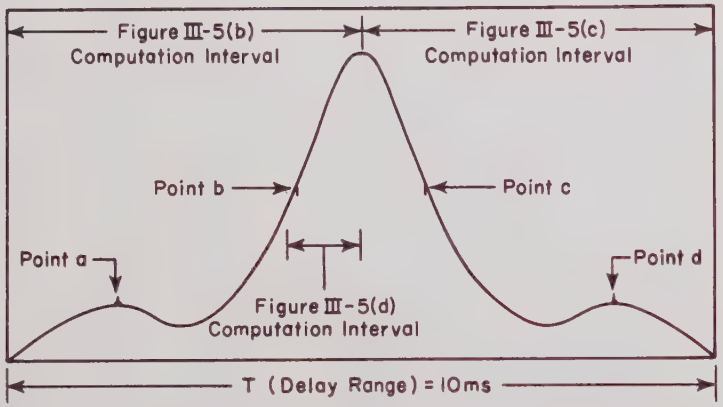


Figure III-5(a). CROSS-CORRELATION FUNCTION COMPUTED WITH MODEL 100.

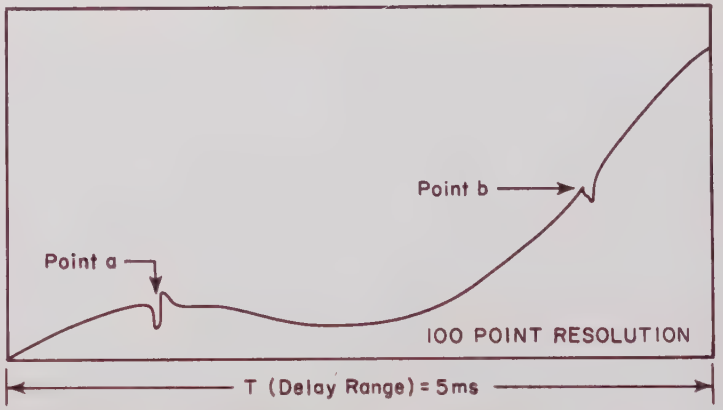


Figure III-5(b). SAME FUNCTION COMPUTED WITH SHORTER DELAY RANGE TO IMPROVE RESOLUTION.

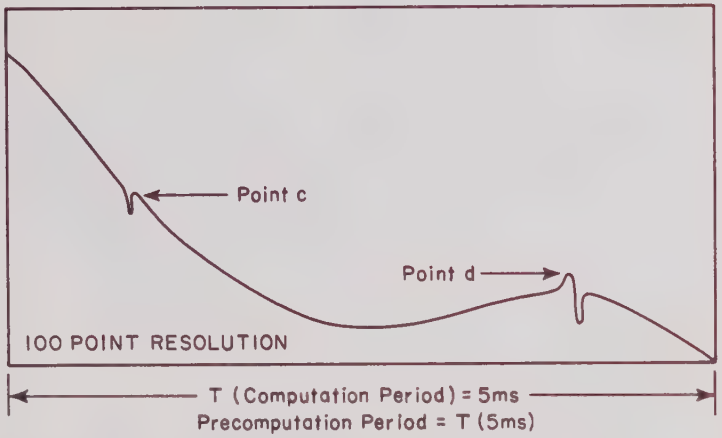


Figure III-5(c). SAME FUNCTION COMPUTED WITH MODEL 101 TO IMPROVE RESOLUTION OF LATTER PORTION OF THE FUNCTION.

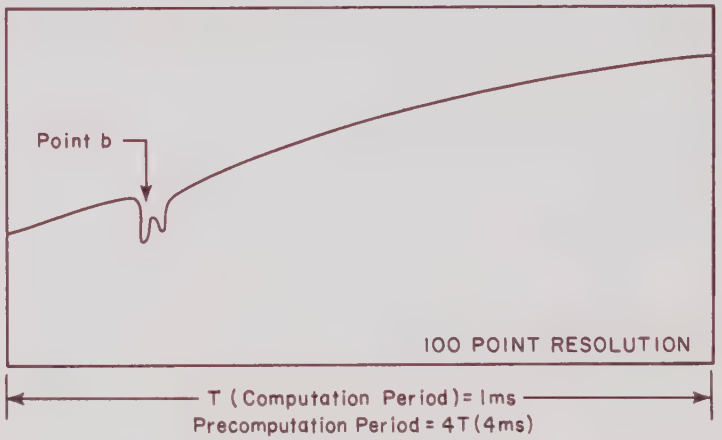


Figure III-5(d). SAME FUNCTION COMPUTED WITH PRECOMPUTATION PERIOD AND COMPUTATION PERIOD SELECTED TO EXPAND SMALL INTERVAL.

Figure III-5. CROSS-CORRELATION EXAMPLE TO ILLUSTRATE RESOLUTION IMPROVEMENT CAPABILITIES OF THE MODEL 101.

tion of the function shown in Figure III-5(a) by choosing the appropriate combination of Precomputation Period and Computation Period.

NOISE, TIME CONSTANT, AND COMPUTATION INTERVAL (Delay Range or Computation Period, according to whether the instrument is a Model 100 or a Model 101)

The final factor to consider in choosing the computation interval is so-called base line noise, that is, false memory contents which mar the correlation function. As this noise depends on both the computation interval and the time constant, Figure III-6, which illustrates the output noise amplitude as a function of these two parameters, has been provided. Observing the figure, note that with most values of integration time constant the noise reaches its minimum value of 1 mV RMS with a computation interval of approximately one millisecond, and that it rises with both shorter and longer computation intervals. With the shortest computation intervals, this noise directly limits how small of a correlation function can be recovered. With long computation intervals, noise is less of a problem because it can be made small by increasing the averaging time constant. Besides affecting the output noise level, the time constant determines the time required to compute the function, five time constants being required for the function to "grow" to within one percent of its final value. Obviously, the improved signal-to-noise ratio obtained by using a very long time constant must be weighed against the additional experimental time required. If the correlator is being gated (see "GATING", page III-23), this time must be multiplied by 1/duty factor. A third factor to be considered in choosing time constant is that in order for a computed correlogram to be accurate, the integrating time constant should be long relative to the period of the lowest frequency component of the input signal(s). By choosing a time constant which is sufficiently large to obtain low output noise, this criterion is automatically met.

As there are 100 separate integrators, the time constant of each being determined by a separate RC network, changing the integrating time constant of the instrument involves changing the time constant of all 100 networks. Each network (there are ten on each of the Computer Boards) comprises one resistor and one capacitor. Because the time constant resistors are mounted on special spring-loaded standoffs which make replacing the resistors a quick and simple process, changing the integration time constant of the instrument is not as difficult as it might first appear. It should be mentioned that as the field effect transistors associated with each averaging circuit are very easily damaged by static discharge, one must take reasonable precautions, as listed on page VII-1, to avoid such discharges through the Computer Boards when changing the Time Constant Resistors. A suitable procedure for changing the time constant follows.

(1) Shut the power off and unplug the line cord.

(2) Remove the top cover. The two screws holding it in place are located underneath the rear edge.

(3) Remove one Computer Board. Note the ten resistors mounted on spring loaded standoffs.

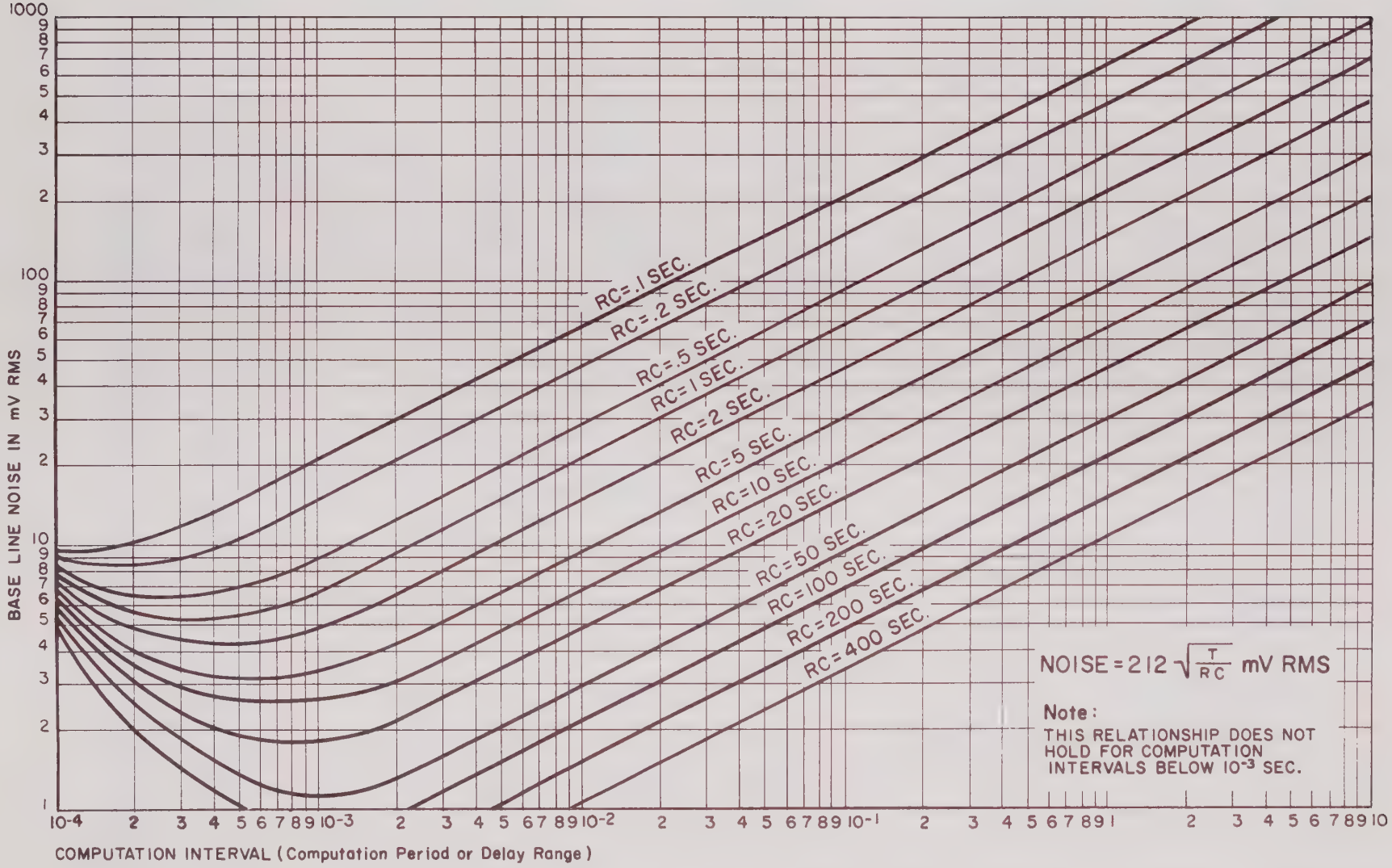


Figure III - 6. TYPICAL BASE LINE NOISE (mV RMS) AS A FUNCTION OF COMPUTATION INTERVAL AND AVERAGING TIME CONSTANT.

(4) Remove these time constant resistors. Pushing down on the standoffs releases the resistors.

(5) Replace the resistors removed in step four with the new time constant resistors. These resistors should be TC/4 megohms, where TC is the desired time constant.

(6) Return the Computer Board to its socket.

(7) Proceed in like manner to change the time constant of all 100 averagers. NOTE: There are two different kinds of Computer Boards. The first type, of which there is one, is identified by the letter "A" next to the guide pin. The second type, of which there are nine, is identified by the letter "B" next to the guide pin. The nine type B boards are freely interchangeable. However, the type A Board is not interchangeable with a type B Board and so must be returned to its own connector.

OPERATION MODE SWITCH

As pointed out earlier, the Operation Mode Switch governs computing and readout. When the switch is in the "COR. $0<\tau<T$" position, the instrument computes the function over the selected computation interval. At the same time, providing the Readout Controls are appropriately set, the "growing" function can be monitored. Placing the switch in the "READOUT ONLY" position halts the computation process. However, the function computed and stored in the memory up to the point of switching to "READOUT ONLY" may be read out in the usual manner. Finally, in the "READ $\tau=0$" mode the instrument computes exactly as in "COR. $0<\tau<T$", the difference between the two modes being that in the former, instead of the entire stored function being available for readout, only the first point is supplied to the output. Because the delay of this point is between zero and one $\Delta\tau$ increment, that is, as nearly zero delay as possible, the output in the "READ $\tau=0$" mode closely approximates the mean square value of an auto-correlated signal, the nearest approximation to that value being obtained when τ has its smallest value or "T" equal 100 microseconds. That this should be so becomes evident when the integral for the auto-correlation function is examined. Ideally, the mean square value is obtained when $\tau=0$, or:

$$C_{ms}(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T f^2(t)\,dt.$$

Practically, the time delay is not quite zero but has a finite value between zero and one $\Delta\tau$ interval. By measuring the mean square value with the 100 microsecond computation interval, the value obtained will represent the average value computed over a period of zero to one microsecond. If the auto-correlated signal contains no predominate frequency components higher than 10 kHz, the difference between the computed and true mean square value will be less than one percent.

METER SWITCH

Located on the front panel are the meter and its associated Meter Switch, which allow monitoring of the correlation output at two different sensitivities as well as monitoring of the time base output. When the Meter Switch is in the "$1V^2$" position, one volt of correlation output will yield full scale meter deflection. When the switch is in the "$4V^2$" position, four volts of output are required for full scale deflection. As full scale output is 3.5 V, full scale deflection of the meter with the Meter Switch in the "$4V^2$" position will never occur. It should be emphasized that the meter indicates the amplitude of only one point of the correlation function or of the time base output. As the memory contents are scanned by the readout circuitry, each pedestal level (or staircase level in the case of the time base output) is connected to the meter in succession. At the slow or medium readout rate, the meter indication will follow the function or staircase. At the fast readout rate, the meter indication cannot follow and will indicate an "average" value of little significance. In general the Meter Switch should be kept in the "OFF" position during fast readout.

With the switch in the "TIME BASE" position, the meter monitors the time base output, and because the time base staircase output voltage rises proportionally to the number of the memory channel being scanned (slow or medium readout rate), the meter indicates to within one channel, which "point" of the correlation function is being applied to the output. One can take advantage of this feature to check the level in any memory channel. To do so one might proceed as follows.

(1) Scan at the slow readout rate (Meter Switch set to "TIME BASE") until the meter indicates the channel of interest has been reached. NOTE: The channel number and meter indication are proportional; a half scale indication means Channel 50 is being scanned; a three-quarters indication means Channel 75 is being scanned, etc.

(2) Quickly transfer the Readout Rate Switch to "STOP" to halt scanning.

(3) Transfer the Meter Switch to one of the two $C(\tau)$ monitor positions to read the level on the particular memory capacitor being sampled.

Because the meter indicates "one point information", it is difficult to evaluate the meter indication when the memory contents are being applied to it sequentially. Consequently, it is usually convenient to keep the Meter Switch in the "OFF" position (disconnected from the correlator circuitry). The meter is particularly useful, however, as an indicator of the mean square value of an auto-correlated function; no scanning beyond the first point occurs when the Operation Mode Switch is set to "READ τ=0".

Another use for the meter is in making a point-by-point plot of a correlation function if a recording instrument is not available. A suitable procedure follows.

(1) Set the Readout Rate and Readout Mode Switches to "STOP" and "SINGLE SWEEP" respectively. With this combination of control settings the memory contents are transferred to the output step-by-step by actua-

ting the Trigger Pushbutton Switch. Except that the Pushbutton is used instead of externally derived pulses, operation is exactly the same as during remote memory transfer, and the reader is referred to "MEMORY TRANSFER", page III-24 for a detailed description of the transfer "program".

(2) Using the Trigger Pushbutton Switch to advance the scanner, read each memory level in succession from the front panel meter. Use that $C(\tau)$ position of the Meter Switch which provides the highest on scale indication.

3.5 READOUT

Any correlation function computed by the Model 100 is stored in the memory as 100 discrete voltage levels or pedestals. When readout takes place, these 100 pedestals are sequentially connected to the Output Jack. Two features of the readout circuitry are: (1) that the readout is nondestructive (within limits), and (2) that the readout rate is completely independent of the computation interval. As a result, regardless of the computation time base, the readout rate appropriate to the recording system available (X-Y recorder, strip-chart recorder, oscilloscope-camera combination) may be used. In addition, readout can take place either after completion of the computation process or simultaneously with it. Three controls govern the readout circuitry. They are the Operation Mode Switch, the Readout Rate Switch, and the Readout Mode Switch.

OPERATION MODE SWITCH

When this switch is in the "COR. $0<\tau<T$" position, computation takes place. Readout is also available if the Readout Rate and Readout Mode Switches are appropriately set. When the switch is in the "READOUT ONLY" position, no computing takes place. Whether or not readout occurs depends again on the Readout Rate and Readout Mode Switches. In the "READ $\tau=0$" position, both computation and readout of the first memory channel take place. If, however, a readout scan of the memory contents is in progress at the time the Operation Mode Switch is placed in the "READ $\tau=0$" position, that scan will finish before the first channel is sampled. Upon reaching the first point, scanning will stop. During "Read $\tau=0$" operation, the first memory level is connected to the Output Connector and the first staircase level (50 mV) is available at the Time Base Connector. It should be pointed out that the "STOP" position of the Readout Rate Switch overrides the Operation Mode Switch. When the Readout Rate Switch is set to "STOP", the scanner cannot advance beyond the point reached when "STOP" was selected; only by chance will the level in the first memory channel be read out. To use the "READ $\tau=0$" position to determine the mean square value of a signal, the Readout Rate Switch should be set to "FAST", the Readout Mode Switch should be set to "CONT.", and the mean square value should be read from the front panel meter with the Meter Switch set to either "$1V^2$" or "$4V^2$", whichever is appropriate.

READOUT RATE

The Readout Rate Switch, as its name implies, determines the rate at which the memory contents are applied to the output. Three different rates are

provided, two to be used when the recording instrument is a recorder and the other when it is an oscilloscope-camera combination. In addition, a "STOP" position is provided, in which memory scanning is halted.

During any readout scan, regardless of the readout rate, one sixth of the total scan time is used to perform internal logic (one twelfth at the beginning and one twelfth at the end). The remaining five sixths of the scan period are used to sequentially apply the 100 consecutive pedestal levels (the memory contents) to the output. Coincident with the memory scanning an output is available at the front panel "TIME BASE" BNC connector. This output is a function of the readout rate; with "SLOW" and "MED." it is a staircase, but with "FAST" it is a pulse.

When the Readout Rate Switch is in the "FAST" position, the scanning rate is two points per millisecond, fifty milliseconds being required to scan the entire memory contents. As a result of the logic requirement mentioned above, the interval from initiation of scan to when it can be repeated is 60 ms, and the readout repetition rate (assuming the Readout Mode Switch is in "CONT.") is 16 and 2/3 readouts per second. The time base output during fast scanning is a fifty millisecond wide pulse exactly coincident with the memory scanning. The pulse baseline is at plus one volt and its peak amplitude is plus twelve volts. When scanning repetitively (Readout Mode Switch set to "CONT."), a ten millisecond gap can be observed between consecutive Time Base Output Pulses. This gap comprises the five millisecond logic period at the end of one readout period and the five millisecond logic period at the beginning of the next. By triggering an oscilloscope from the leading edge of the Time Base Pulse and using a horizontal sweep time of five ms/cm (assuming a ten centimeter trace length) the memory contents will be optimally displayed for monitoring or recording the correlation function.

With the Readout Rate Switch set to "MED." the readout rate is twelve points per second and approximately eight seconds are required to scan the memory once. Allowing for the logic time, one complete readout period lasts ten seconds. With the switch set to "SLOW" the readout rate is reduced to its minimum value of two points per second; 50 seconds are required to actually scan the memory contents and ten seconds are required to perform the logic functions. Both of these readout rates are intended for use when the recording instrument is either a strip-chart or X-Y recorder. In general, the medium rate is used in "setting up" the recorder, and the slow rate is used to actually record the correlation function. With either of these two readout rates the time base signal is a positive going, zero to five volt staircase, which is coincident with the memory scanning. This 100 step "staircase" is particularly well suited for driving one axis of an X-Y recorder, and the correlogram obtained will be "point-to-point", providing the recorder frequency response is the same for both axes.

The final position of the Readout Rate Switch is the "STOP" position. In this position the memory cannot advance, except by depressing the Trigger Pushbutton Switch, which advances the scanner one step at a time. "STOP" overrides both the Operation Mode and Readout Mode Switches. Also, for the duration that the Readout Rate Switch is in the stop position, the time base output "holds". The stop position is used in monitoring the contents of any one channel and in setting the horizontal and vertical deflection sensitiv-

ities of a recorder. Monitoring the time base output with the front panel meter facilitates monitoring a specific channel. For example, a half scale indication with the Meter Switch in "TIME BASE" would indicate that Channel 50 is being monitored. To actually measure the level on Channel 50, the Meter Switch should then be transferred to "$1V^2$" or "$4V^2$", as appropriate.

READOUT MODE

The Readout Mode Switch allows selection of any one of the three readout modes, "CONT.", "SINGLE SWEEP", and "ERASE". When the Readout Mode Switch is in the "CONT." position, readout scans are repetitive; as soon as one readout scan ends another begins. However, this repetitive scanning is subject to override by the Readout Rate Switch in "STOP" and by the Operation Mode Switch in "READ τ=0". Continuous operation is usually used in conjunction with the fast readout rate to monitor or record the memory contents when using an oscilloscope.

In the single sweep position one must depress the "TRIGGER" Pushbutton Switch to initiate a scan. If a scan is already in progress when the Readout Mode Switch is placed in the single sweep position, that scan will finish before another can be initiated. The "READY" Light, located directly above the Trigger Pushbutton, indicates that the scanner is receptive to triggering. Upon depressing the pushbutton, a readout scan begins and the Ready Light goes out. Only after the initiated scan is completed does the Ready Light come on again. Single sweep operation is usually used when the recording instrument is a strip-chart or X-Y recorder. As in the case of the Continuous Readout Mode, scanning in the Single Sweep Mode is subject to override by the "STOP" position of the Readout Rate Switch. With this combination scanning will advance one step each time the Trigger Pushbutton is depressed. A special case is that of "SINGLE SWEEP" and "READ τ=0". With this combination it is not necessary to use the Trigger Pushbutton to advance to the first memory channel. As soon as the Operation Mode Switch is placed in the "READ τ=0" position, the memory scanner advances to the first computation point (providing the Readout Rate Switch is not set to "STOP"). Switching back to either of the other two positions of the Operation Mode Switch (Readout Only or Continuous) will initiate the complete scan.

The last position of the Readout Mode Switch is "ERASE", in which the contents of the memory are reduced to zero in about five seconds, regardless of the position of the Readout Rate Switch (other than "STOP", which exercises its usual override inhibiting of the scanner). If the Operation Mode Switch is in "READ τ=0", only the first memory channel will be erased; for erasing of all 100 stages the Operation Mode Switch must be in one of the other two positions.

It might be mentioned that the time base output in the Erase Mode depends on the readout rate selected. With a combination of "ERASE" and "FAST", the fast readout rate pulse is available at the time base output connector. This pulse can be used to trigger an oscilloscope which is monitoring the "erasure" of the correlation function. When erasing at the "SLOW" or "MED." readout rate (and of course "STOP"), the time base output is grounded.

MEMORY AND READOUT RESTRICTIONS

Although the instrument features non-destructive readout of its 100 channel capacitive analog memory, certain restrictions must be observed, both with respect to the memory "storage time" and with respect to the number of times readout can take place to assure negligible degradation to a stored function. Two factors determine these restrictions. The first is simple "leaking away" of the stored information, and the second is level shifting caused by capacitive and rectification effects in the memory and memory scanner circuitry. By basing the restrictions on a degradation to the stored waveform of approximately one percent of full scale, limits commensurate with general instrument performance are obtained. The memory hold time limit is ten minutes and is based on the fact that the displacement of the voltage level on any memory capacitor from its level at the beginning of the hold period will not exceed 30 mV in ten minutes at 25°C. At higher temperatures greater leakage can be expected. It should be pointed out, however, that this is a worst case specification; the level on most memory capacitors will change much less than 30 mV in ten minutes. As for readout scanning degradation, the limit is 1000 readout scans for no more than 30 mV shift in any pedestal level. Obviously readout scanning degradation does not contribute significantly unless one is using the fast readout rate. If one is using the fast readout rate, however, 1000 sweeps are accumulated in one minute, and unnecessarily prolonged operation at the fast rate should be avoided. In any case, both restrictions apply only when the Operation Mode Switch is set to "READOUT ONLY".

3.6 RECORDING

The versatility of PAR Signal Correlators allows the operator the choice of any one of three recording instruments, strip-chart recorder, X-Y recorder, or oscilloscope-camera combination. As the factors to be considered for each vary somewhat, they will be treated separately.

STRIP-CHART RECORDERS

Strip-chart recorders are of two basic types, galvanometric and servo. Galvanometric recorders are current-sensing devices and typically require either 0.5 mA or 1.0 mA for full scale deflection. To drive such a recorder from the correlation output BNC connector (output impedance 1 kilohm), one must usually insert a resistor between the output of the Correlator and the input of the recorder if full scale correlator output is to yield no more than full scale recorder deflection. The value of the resistor will, of course, depend on the resistance and on the sensitivity of the galvanometer. For 0.5 mA for full scale deflection recorders, the series resistance in kilohms should be about 6-R, where "R" is the galvanometer resistance in kilohms. For 1.0 mA recorders the resistor should be 2.5-R kilohms. With the calculated resistance installed, the recorder sensitivity can be calibrated by checking the deflection of the recorder against the deflection of the front panel meter. As it is to one's advantage to use as much of the dynamic range of a recording device as possible, a smaller series resistor or even no series resistor at all may be more suitable if the computed function is of low amplitude. Because galvanometric recorders are usually "slow", having a time constant which typically is between 0.1 and 1.0 second, it is advisable to use only the "SLOW" readout rate when driving this type of recorder. A chart

drive speed of roughly six inches per minute will yield a good quality correlogram.

Servo type chart recorders are usually voltage-sensing devices with a wide range of deflection sensitivities; it is seldom necessary to insert additional series or shunt resistors to make them compatible with the Correlator Output. As they are frequently faster than galvanometric type recorders, it may be possible to use the medium readout speed (twelve points per second) and a faster chart speed, one inch per second being about right.

X-Y RECORDERS

X-Y recorders differ from strip-chart recorders in that they require not only an "information" signal, but a drive signal as well (although a few X-Y recorders have internal time base capabilities). Since the correlator time base output is synchronous with the readout of the correlation function, it is particularly well suited to driving the X axis of an X-Y recorder. The time base output signal is a staircase which starts at zero and increases to plus five volts in 100 equal steps, the last step and the 100th point of the correlation function being coincident.

The X-Y plot should be made either at the slow or medium readout rate (the choice being determined by the frequency response of the recorder) and with the Readout Mode Switch in the single sweep position. The rear panel Smoothing Switch should be set to "ON" to equalize the "X" and "Y" frequency response of the correlator. Each time the Trigger Pushbutton is depressed, the following sequence takes place.

(1) While the time base output is still at zero level, the memory scanner begins to monitor the first memory channel. As a result, providing the stored function has a non-zero value at the first point, a vertical trace at the beginning of the chart results.

(2) The pen remains at this first point for about 8 percent of the total readout period; for this interval the time base output remains at zero.

(3) Scanning of the remaining 99 memory channels and stepping of the time base staircase commence. Both advance "in step".

(4) Immediately after the last point is recorded the correlation output is switched to ground while the time base output remains at its maximum value. Providing the function has a non-zero value at the last point, a vertical trace is produced at the end of the correlogram.

(5) The pen remains at this point for about 8 percent of the total readout period; for this duration the time base output holds its maximum value.

(6) The time base output resets to zero, and, because the Y axis signal is already at zero (step four), a horizontal zero level retrace to the origin occurs. It is not necessary to lift the pen to prevent the retrace line from marring the correlogram during reset.

The "STOP" feature provided by the Readout Rate Switch facilitates setting the recorder deflection sensitivity controls. A procedure suitable for setting up the recorder controls follows.

(1) If the input signals are continuously available, set the Operation Mode Switch to "COR. $0<\tau<T$". If they are not, set the switch to "READOUT ONLY".

(2) Set the recorder zero controls for no horizontal or vertical deflection.

(3) Depress the Trigger Pushbutton to start a readout scan.

(4) As soon as the tracing of the function is completed but before horizontal retrace occurs (step six in the preceding procedure), place the Readout Rate Switch in the "STOP" position, thereby stopping the scanner and allowing as much time as necessary to adjust the horizontal deflection sensitivity.

(5) Adjust the recorder horizontal deflection sensitivity for full scale deflection.

(6) By examining the amplitude of the "trial trace", determine the appropriate vertical deflection sensitivity and adjust as indicated.

(7) Transfer the Readout Rate Switch from "STOP" to one of the other two positions. Horizontal retrace will take place restoring the quiescent state.

Although the ten minutes for one percent degradation specification allows ample time for properly calibrating a recorder while operating in the Readout Only Mode, it is always to one's advantage to perform all readout functions, including recorder calibration, while computing in the "COR. $0<\tau<T$" Mode; no degrading of the memory contents can occur as long as the input signals are available.

As a result of the drive signal being a staircase and the information signal being a series of pedestals, the correlogram obtained will be drawn point-to-point, providing that the horizontal and vertical frequency response of the recorder are the same. If they are not the same, the plot will be "stepped" instead of smooth, and in extreme cases, the recorder may even draw a loop around each point. If a "rough" plot is obtained, adjust the frequency response as required to obtain the point-to-point correlogram. Controls for this purpose are provided on most recorders.

Figure III-7 shows two correlograms plotted with an X-Y recorder. The upper plot is that of a correlogram obtained with a recorder having an equal horizontal and vertical frequency response. The lower plot was made with a sharply reduced X axis frequency response.

Note that Figure III-7 illustrates the readout program. Both plots have a vertical trace at the beginning and at the end of the trace, and a zero level retrace. Also note that the trace begins with a "plateau". This "plateau"

X AND Y FREQUENCY RESPONSE EQUAL

X FREQUENCY RESPONSE SLOWER THAN Y FREQUENCY RESPONSE

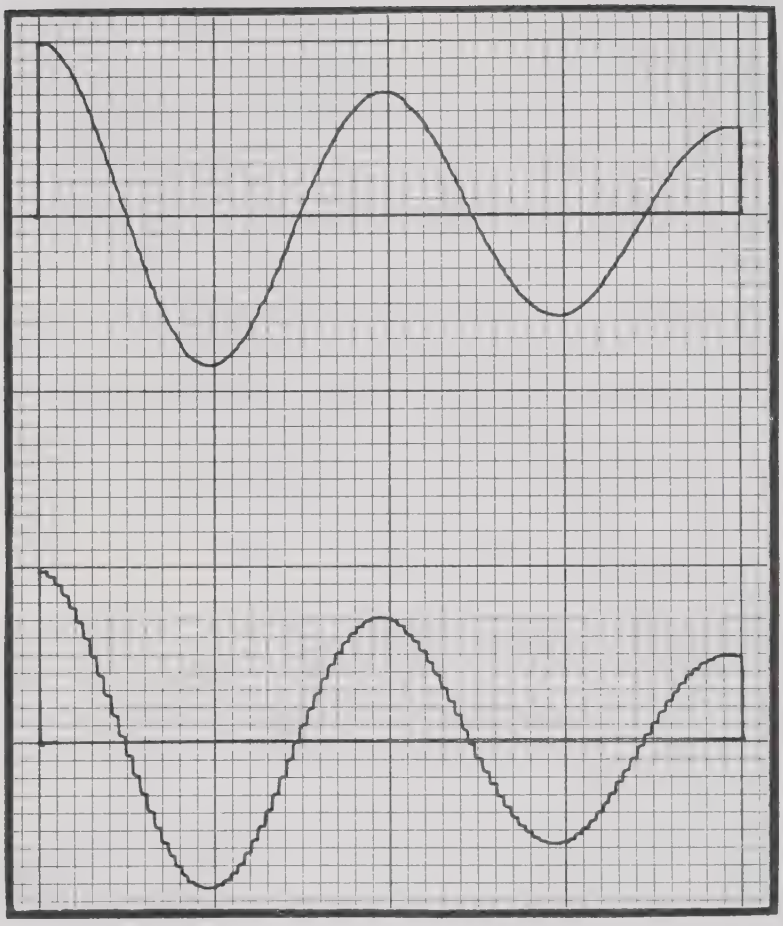


Figure III-7. X-Y PLOTS SHOWING EFFECTS OF FREQUENCY RESPONSE MISMATCH

is a normal function of the readout program. The initial level is obtained because sampling of the first memory channel begins before stepping of the X axis drive "staircase". When the first step takes place, a 1% of time base duration plateau at the level of the first memory channel occurs to begin the correlogram plot.

OSCILLOSCOPE-CAMERA

The first point to be made is that oscilloscope-camera recording is done at the fast readout rate. The second is that one ought to operate continuously no longer than necessary in the Readout Only Mode at the fast readout rate, because the 1000 sweeps for 1% degradation limit is reached in one minute. If the picture is taken while still computing, as is possible by continuing the experiment beyond the five time constants required and leaving the Operation Mode Switch in the "COR. $0<\tau<T$" position, the 1000 sweep limit does not apply, and the operator can set his camera and oscilloscope controls at a somewhat more leisurely pace than would otherwise be the case. Another solution is to keep the Readout Mode Switch in the "SINGLE SWEEP" position, trans-

ferring it to the "CONT." position only as long as necessary to take the picture. Some operators may prefer to photograph a single sweep to eliminate any error resulting from "trigger jitter".

The time base output at the fast readout rate is a positive one-to-twelve volt pulse, synchronous with the correlation output. By triggering the oscilloscope from the leading edge of the pulse and setting the sweep time to five milliseconds per cm (assuming a ten cm trace length), the memory contents will exactly fill the screen. Whether or not the correlation function is optimally located in the memory depends on the computation interval, and, in the case of the Model 101, on the Precomputation Period. Frequently it may be advantageous to compute the function at several different computation intervals, making a separate record of each. If the correlation function is not located as desired, do not change the oscilloscope sweep speed but instead recompute the function with a different computation interval or Precomputation Period. The optimum vertical deflection sensitivity is easily determined by examining the function for a few seconds with the oscilloscope.

SMOOTHING

A correlation function is stored in the memory as a series of discrete voltage levels or pedestals. With slow or medium readout rate recording with a strip-chart recorder, the correlogram obtained will clearly show the individual pedestals. The situation is the same for an X-Y recorder, except that the correlogram will have a point-to-point appearance due to the staircase nature of the time base output. At the fast readout rate, however, one has the option of photographing the signal exactly as it is stored, as a series of discrete voltage levels, or, by placing the rear panel "SMOOTHING" Switch in the "ON" position, as a smooth continuous function with negligible loss of detail or amplitude.

3.7 REMOTE PROGRAMMING

Under certain experimental conditions the remote programming capabilities of the Correlator can be of great value. Among the functions which can be controlled remotely are computing, erasing, and transfer of the memory contents to another computer for further processing. All of these functions are achieved by applying appropriate control pulses to the proper pins of the rear panel Interface Connector, J1. Table III-1 indicates the required pulse levels and the pins to which they must be supplied. In addition to these command signal lines, other correlator output signal lines are brought out at J1. The "on" and "off" signal and load levels of each, along with the associated impedances, are all indicated in Table III-1.

GATING

Gating the correlator, that is, computing the function only over certain specific intervals, is accomplished by applying appropriately timed gating pulses to pin L of J1. For the duration of each pulse the correlator is transferred to readout only operation and computing stops. To compute over a specific interval the COMPUTE INHIBIT "OFF" command level (see Table III-1) must be applied to pin L over that interval. This "compute" command must be synchronized with the signal(s) to be correlated and must bracket them in

time. For the remaining time the COMPUTE INHIBIT "ON" command level must be applied.

Gated operation with low duty factor signals results in higher amplitude correlation functions and hence better signal-to-noise ratios than would be obtained by not gating. This improvement in amplitude, which is inversely proportional to the duty factor, takes place because the zero level input over the interval of no signal is not averaged.

Two factors to be considered during gated operation are the time required to compute the correlation function and leakage degradation during computation. Normally, five times the integration time constant are required for the computed function to "grow" to within one percent of its final value. With gated operation, however, this time is increased by a factor of 1/duty factor. With reference to leakage degradation, so long as the duty factor is no smaller than 16×10^{-4} TC, where "TC" is the integrating time constant, the leakage degradation when computing will not exceed 1%.

MEMORY TRANSFER

The first requirement to transferring information from the correlator memory to that of a computer is that the two instruments be synchronized, that is, the individual voltage levels which constitute the memory contents must be sequentially transferred, in step, at a rate which is acceptable to both instruments. In the case of the Correlator, external remote control of the memory scanning circuitry is accomplished by applying a series of pulses to pin H of J1. Each pulse will advance the scanner one step, and the memory contents will be applied to the front panel correlation output BNC connector at the repetition rate. The maximum acceptable pulse repetition rate is 120 repetitions per second, which allows the transfer to be completed in one second. There is no lower limit. Usually, some sort of "interface" device will be required between the two instruments.

With the Readout Mode Switch set to "SINGLE SWEEP" and the Readout Rate Switch set to "STOP", the memory scanner can be advanced step-by-step either by applying the appropriate pulses to pin H of J1 (see Table III-1), or by depressing the front panel Trigger Pushbutton (once for each "step"). In the quiescent state the output connector is at ground potential. Upon application of the first scan pulse the first memory channel is connected to the output. The first memory channel continues to be applied to the output for pulses two through ten. Beginning with the eleventh pulse the memory channels are consecutively connected to the output. The eleventh pulse connects channel two, the twelfth connects channel three, etc., up to the 109th pulse which connects memory channel 100. With the 110th pulse the output connector is again placed at ground potential, where it remains for pulses 111 through 119. Pulse 120 restores the quiescent state, that is, the state in which the next pulse will connect memory channel one to the output. As it may be convenient to gate the external equipment, a suitable Start/Finish Output is available at pin F of J1. Quiescently the potential at pin F is plus one volt. It remains at that potential during pulses one through nine, but rises to plus twelve volts when the tenth pulse is applied. This twelve volt level lasts until the 110th pulse, at which time the one volt level is restored. By using the pin F output as a gate signal, the level on memory channel one can

PIN	SIGNALS	CIRCUIT IMPEDANCE		PROGRAMMING VOLTAGE LEVELS REQUIRED		OUTPUT SIGNAL LEVELS AND MAX. LOAD LIMITS				REMARKS
						ON		OFF		
		ON	OFF	TO TURN ON	TO TURN OFF	SIG.	LOAD	SIG.	LOAD	
L	COMPUTATION INHIBIT	10 k	reverse biased diode	+0.5 V to -12 V	+5 V to +100 V or open					Similar to Front Panel READOUT ONLY function.
H	READOUT ADVANCE	10 k	reverse biased diode	-0.5 V to +12 V	-5 V to -100 V or open					
D	ERASE COMMAND	10 k	reverse biased diode	+0.5 V to -12 V	+12 V to +100 V or open					
A	GROUND REFERENCE									
N	"B" OVERLOAD SIGNAL	100 Ω	600 Ω			+1 V	10 mA	+24 V	10 mA	
K	READOUT CLOCK OUTPUT	2 k	2 k			-1 V	1 mA	-11 V	1 mA	Clock load must be returned to negative voltage.
F	START/FINISH SIGNAL OUTPUT	20 k	1 k			+12 V	½ mA	+1 V	½ mA	
R	+12 V SUPPLY OUTPUT									Maximum load is is 100 mA.
B	+24 V SUPPLY OUTPUT									Maximum load is is 50 mA.
C	-24 V SUPPLY OUTPUT									Maximum load is is 50 mA.

Table III-1. INTERFACE CONNECTOR (J-1) SIGNALS AND LEVELS

be "sampled" no longer than the level on each of the other channels. The relationships indicated in this paragraph are shown in Table III-2.

PULSE	PEDESTAL SAMPLED	LEVEL AT PIN F OF J1
Quiescent	None (output zero)	+1 V
1 - 9	1	+1 V
10 - 109	1 - 100	+12 V
110 - 119	None (output zero)	+1 V
120 (quiescent)	None (output zero)	+1 V

Table III-2. START/FINISH AND C(τ) OUTPUTS DURING MEMORY TRANSFER

REMOTE TRIGGERING

If the Readout Mode Switch is set to "SINGLE SWEEP" and the Readout Rate Switch set to some position other than "STOP", applying the specified level to pin H will trigger a single sweep. This is completely equivalent to pushing the front panel Trigger Pushbutton during "normal" Single Sweep operation, as discussed under "READOUT MODE", page III-18.

ERASE

To erase remotely, the Erase Command as specified in Table III-1 must be applied to pin D of J1 and the memory scanner must be stepping. Because the time constant of the erase circuit is about four milliseconds and only one memory channel can be connected to the erase circuit at a time, each of the 100 memory channels must be connected to the erase circuit for five time constants or 20 milliseconds. Erasing will be fastest when the repetition rate of the scan pulses applied to pin H is at least 50 repetitions per second. With slower stepping rates, each memory channel will be erased longer than necessary to reduce the memory contents to the level of the base line noise. With repetition rates of fifty repetitions per second but less than the maximum of 120 repetitions per second, approximately three seconds are required to erase. As the erase time constant is much smaller than the integration time constant, one could erase while computing if such a need should arise. It should be mentioned that with remote erasing the time base output signal is the staircase and not the fast readout rate pulse.

SECTION IV
SOME APPLICATIONS OF AUTO- AND CROSS-CORRELATION MEASUREMENTS TO SCIENCE AND ENGINEERING

4.1 INTRODUCTION

In recent years scientists and engineers have become increasingly aware that they must be concerned with modern information and communication theory. This has become necessary because most experimental work has pushed the sensitivity and accuracy of measurements to the point where noise, due to both thermal fluctuations and environmental interference, is the limiting factor. This is true not only in such obvious fields as radio astronomy, but is also the case in research in neurology, seismology, solid state physics, etc.

Perhaps the first historical instance where the need for modern information theory techniques arose was at the end of the last century, when it was found that galvanometers were limited in their ultimate sensitivity by Brownian fluctuations. It was soon noted by the early experimentalists that a greater ultimate sensitivity could be achieved by making the galvanometer have a longer period -- probably the first case where the bandwidth was narrowed to improve on signal-to-noise ratio! In today's experimental work, coping with noise generally requires a far more subtle approach than just increasing the detecting instrument's period.

The impact that the discovery of Hertzian waves had on engineering and science was remarkable. In the attempt to provide a workable theoretical basis for radio, linear systems were assumed and extensive use was made of the methods of Fourier, Heaviside, etc., to describe the behavior of linear systems under periodic or transient excitation. The techniques evolved, those of idealizing to a linear system driven by periodic or almost periodic disturbances, spread beyond the communications area into other branches of science and engineering. Implicit in these techniques was the characterization of signals and information by time functions and their Fourier transforms, i.e., frequency spectra. Even noise was treated as a periodic or a transient phenomenon, whichever was most reasonable. The success of these techniques is not to be denied, as witnessed by the explosive growth of the industries based on these precepts.

However, the limitations of these classical approaches ultimately becomes apparent. In particular, in the study of hydrodynamic diffusion and turbulence, the a option of a linear model excited by periodic disturbances was found to be totally unacceptable, as these phenomena are random processes arising from purely non-linear behavior. In 1920, G. I. Taylor[1] working in England made what was perhaps the first application of correlation analysis for the characterization of random processes. In the years following he made extensive use of correlation concepts in his classic works on diffusion and turbulence. This early work was followed by the rigorous mathematical devel-

[1] G. I. Taylor, Diffusion by Continuous Movements, Proc. London Math. Soc. 20, 196 (1920).

opment of these concepts, notably by Norbert Wiener, who in 1942 wrote a report, The Extrapolation, Interpolation and Smoothing of Stationary Time Series with Engineering Applications[2]. This work had great impact and largely laid the foundation of modern information and statistical communication theory.

4.2 AUTO- AND CROSS-CORRELATION FUNCTIONS

Basic to the characterization of signals and random processes, according to modern theory, are the auto- and cross-correlation functions.[3] They are to modern theory what frequency spectra are to the classical theory. Unfortunately, for most people the correlation functions do not have the intuitive meaning that frequency spectra have, perhaps due to early exposure in life to tuning radios. Let us examine the nature of these concepts on a non-rigorous basis and try to establish a working relationship with them.

Assume that we have some physical process that in various channels gives rise simultaneously to signals $f_A(t)$, $f_B(t)$, $f_C(t)$, etc. Assume further that the physical process is not changing its character with time; i.e., the batteries are not running down, parts are not wearing out, etc.; that we have a stationary situation. Further assume the time functions $f_n(t)$ are not zero, nor do they have a DC component. The signals may be simple or complex periodic waves or they may have the character of noise; that is, randomly varying. Now imagine that we pass one of the signals, say $f_A(t)$, through a perfect delay line which introduces a non-dispersive variable delay of amount τ. We now have available the signal $f_A(t-\tau)$, identical to $f_A(t)$ but just delayed in time. If, as shown in Figure IV-1, we multiply the instantaneous value of $f_A(t)$ by the value of $f_A(t-\tau)$ and obtain the average of the product over a sufficiently long time, we arrive at a quantity which has the following properties.

(1) The product will be a maximum at $\tau=0$.

(2) The value at $\tau=0$ is related to the total power of the signal. If $f_A(t)$ is a voltage, then the average of the product for $\tau=0$ is simply $f_A^2(t)$, or the power the signal will dissipate in a one ohm resistor.

(3) The average value of the product will be a function of τ, the form of which will be characteristic of the original signal, $f_A(t)$.

(4) If the averaging time is long compared to the reciprocal of the lowest frequencies present in $f_A(t)$, then repetitions of the measurement for a given τ will give values very close to one another.

(5) The average value of the product for a negative value of τ is identical to that for the same positive τ.

---

[2]Published in 1949 by John Wiley & Sons.

[3]An excellent account of the details of this subject is given by Y. W. Lee in Statistical Theory of Communication. John Wiley & Sons, 1960, New York.

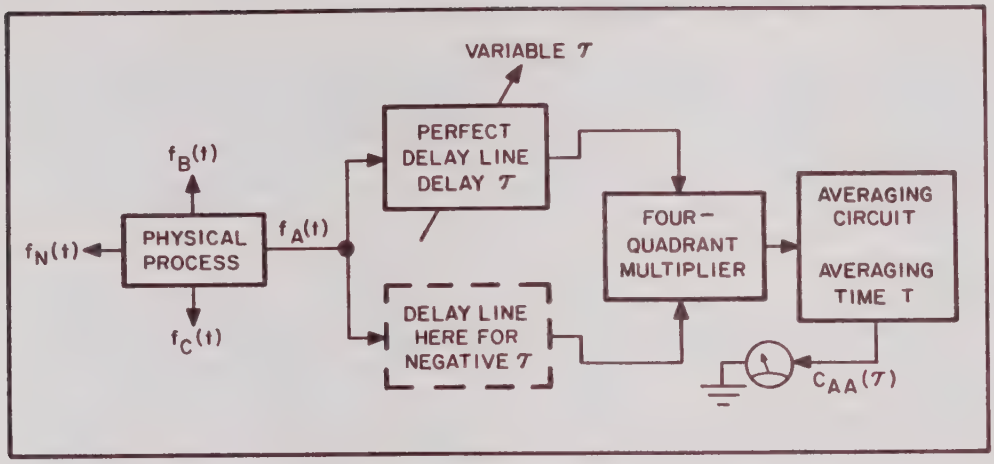


Figure IV-1. BLOCK DIAGRAM OF AUTO-CORRELATOR

In words, we have now described the auto-correlation function for any time function, $f_A(t)$ which is rigorously defined as:

$$C_{AA}(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} f_A(t)\, f_A(t-\tau)\, dt. \qquad (1)$$

Consider what information the function $C_{AA}(\tau)$ can give about $f_A(t)$. First compare $f_A(t)$ with $f_A(t-\tau)$ for very large values of τ. Any physically realizable process that might give rise to a signal will be such that the value of the signal at time t will become more independent of the value at $t-\tau$ as τ grows larger. This will be true even of the oscillators in the most stable atomic clocks. Thermal noise, and even the uncertainty relationship, will eventually introduce randomness that will cause a gradual loss of coherence in the output signal. Hence, we see that for a signal arising from real processes, $C_{AA}(\tau)$ will tend to zero as τ becomes sufficiently large. The value of τ that gives a significant diminuation of $C_{AA}(\tau)$ is a measure of the coherence time of the original signal, and the coherence time of a physical process is an important quantity in its characterization.

An obvious case to mention here is random noise. The auto-correlation function for very wide bandwidth, uniform (white) noise of RMS value E_m is an impulse function at $\tau=0$ of amplitude E_m^2. This tells us that a characteristic of wide band noise is that the value of the signal at any instant is completely independent of the value the instant before and after, in other words, that the coherence time of the process giving rise to the noise is very short.

A property of the auto-correlation function that is not so obvious is given by the pair of reciprocal relations, first rigorously established by Wiener. They are:

$$\Phi_{AA}(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} C_{AA}(\tau)\, \cos\omega\tau\, d\tau \qquad (2)$$

$$C_{AA}(\tau) = \int_{-\infty}^{\infty} \Phi_{AA}(\omega) \cos\omega\tau \, d\omega \qquad (3)$$

These expressions are recognizable as the cosine Fourier transform pair. It can be shown that $\Phi_{AA}(\omega)$, the cosine Fourier transform of the auto-correlation function, is identically the power density spectrum of $f_A(t)$. Hence, an experimental determination of the auto-correlation or of the Fourier density spectrum are completely equivalent, equations (2) and (3) being used for transforming from one to the other.

Traditionally, in experimental work the measurement of the power density spectra of a complex signal has been the preferred way of obtaining information for characterizing the signal. Two reasons for this are: first, the relatively straightforward construction of a wave analyzer and, second, the paramount importance of spectra in specifying the frequency response of equipment needed to handle the signal. However, in certain circumstances, such as in the important case of searching for an unknown coherent signal buried in random noise, the auto-correlation method would probably be the better choice, because the presence of the signal would be detected sooner. The auto-correlation functions for a few representative time functions are given in Table IV-1.

While determining the auto-correlation time function of a signal is in every respect equivalent to the traditional technique of power density spectra analysis, there is no classical analog for cross-correlation analysis. In cross-correlation we are concerned with investigating the nature of the relationship between two signals that arise in some common process. The cross-correlation function is obtained by averaging the product of a time function with a delayed replica of a second time function, as is shown in Figure IV-2.

Formally, the cross-correlation function is defined by:

$$C_{AB}(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{+T} f_A(t) f_B(t-\tau) \, dt. \qquad (4)$$

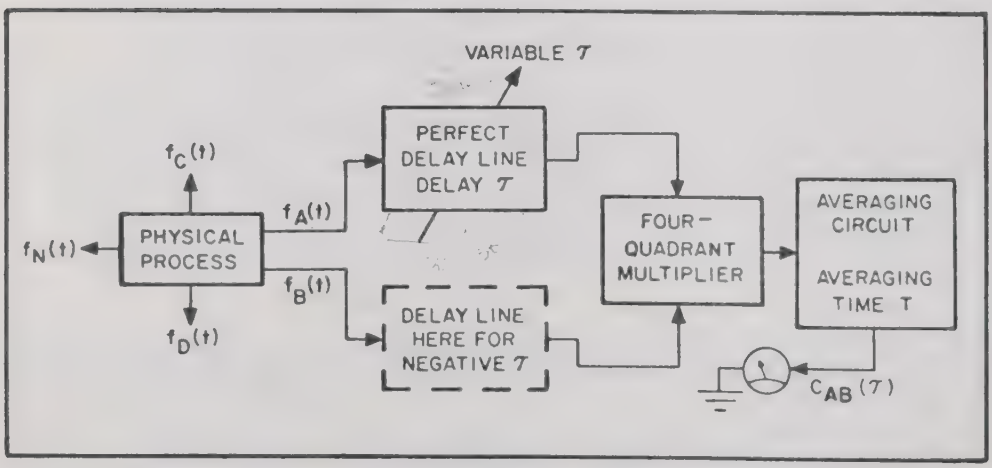


Figure IV-2. BLOCK DIAGRAM OF CROSS-CORRELATOR

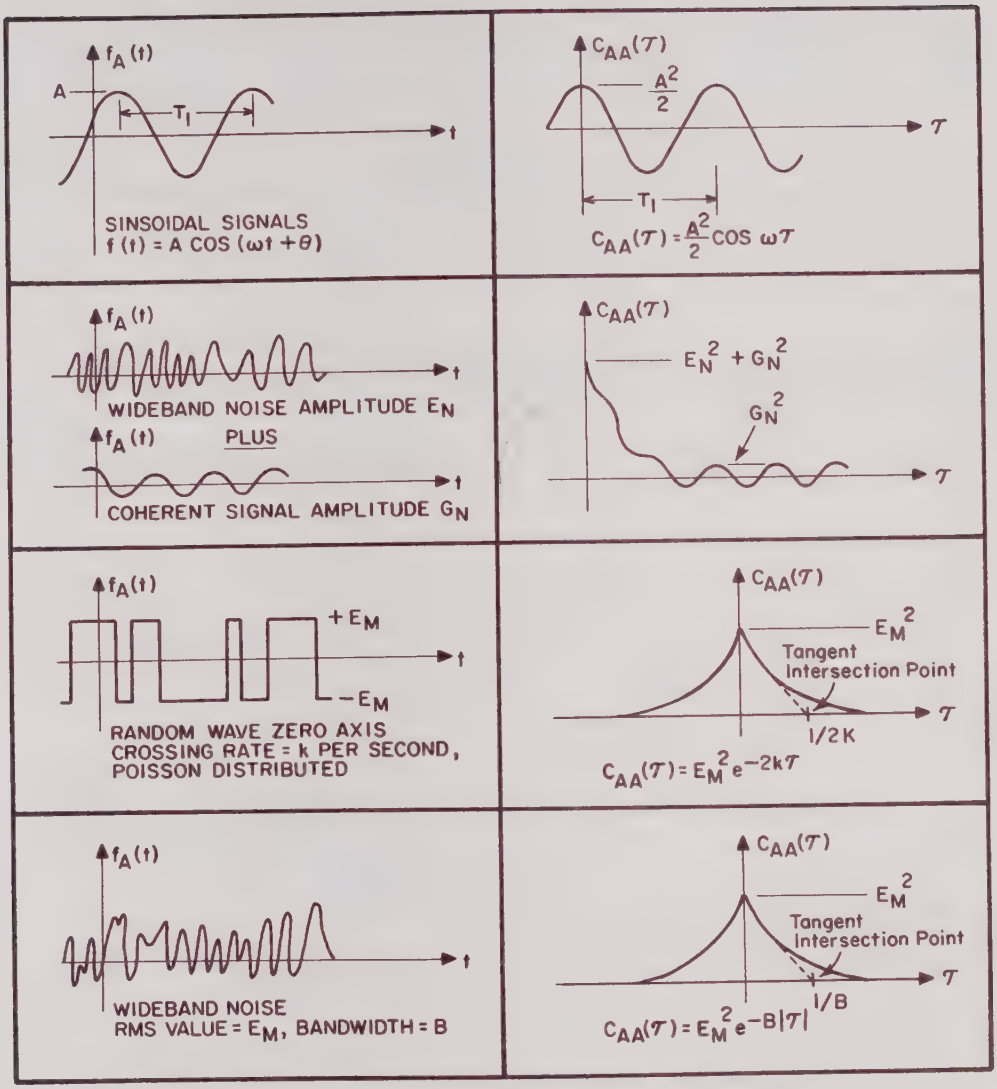


Table IV-1. SOME AUTO-CORRELATION FUNCTIONS

The properties of $C_{AB}(\tau)$ are, in general, quite different from those of the auto-correlation function. For example, $C_{AB}(\tau)$ is not equal to $C_{AB}(-\tau)$. However, it should be clear that $C_{AB}(-\tau) = C_{BA}(\tau)$, a result of great practical importance in obtaining $C_{AB}(\tau)$ for negative values of τ. In practice, as in the case of auto-correlation operation, the averaging process indicated in equation (4) need only be extended for times long compared to the longest period present in signals $f_A(t)$ and $f_B(t)$. Also, for signals that arise from real physical processes, noise and the uncertainty principle will assure that $C_{AB}(\tau) \to 0$ as $\tau \to \infty$.

The cross-correlation function can be described as representing the degree of conformity between two signals as a function of their mutual delay.

Hence, if $f_A(\tau)$ and $f_B(\tau)$ arise from two completely separate processes, then $C_{AB}(\tau)=0$. As in the case of the auto-correlation function, we can again define a reciprocal Fourier pair.

$$\Phi_{AB}(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} C_{AB}(\tau)e^{-j\omega\tau}d\tau \tag{5}$$

$$C_{AB}(\tau) = \int_{-\infty}^{\infty} \Phi_{AB}(\omega)e^{j\omega\tau}d\omega \tag{6}$$

In this case, however, the physical meaning of $\Phi_{AB}(\omega)$ is not so clear. We shall call it, following Lee,[3] the spectrum of cross-correlation of $f_A(t)$ and $f_B(t)$.

The method of cross-correlation analysis of two signals provides a powerful

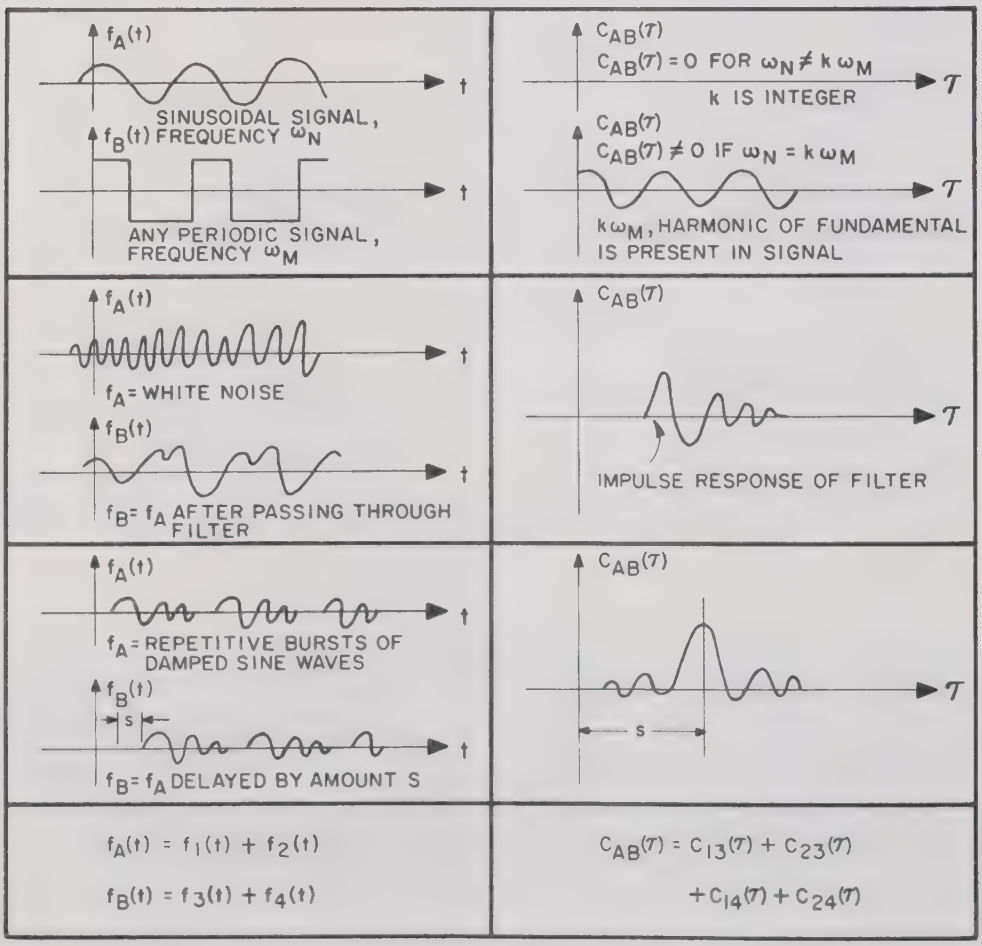


Table IV-2. SOME CROSS-CORRELATION FUNCTIONS

analytical tool that far transcends any technique available in classical communication theory. The ability to measure the alikeness of two signals that might arise from a common physical phenomenon as a function of their relative delay is generally capable of providing a much deeper insight into the phenomenon than any analysis of the properties of either or both of the signals separately. Why this might be so can be inferred by an examination of Table IV-2, which shows a few examples of cross-correlation between various typical waveforms. Note that the fourth (no waveform provided) example describes the general case and is not intended to specifically apply to one of the three associated examples.

An example of the application of cross correlation to a specific problem may help to clarify the nature of the technique. As an example, consider one of the earliest applications made of cross-correlation, the study of hydrodynamic turbulence. If two velocity responding probes are inserted in a stream of fluid undergoing turbulent flow and the cross-correlation function obtained

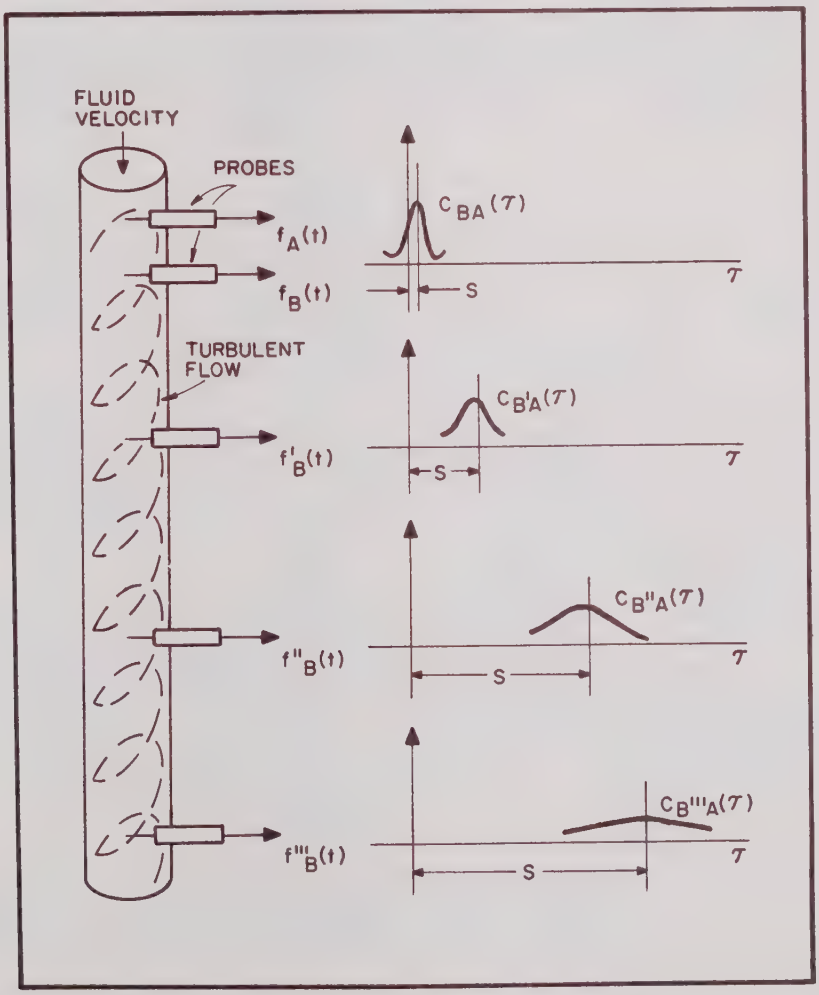


Figure IV-3. CROSS-CORRELATION IN HYDRODYNAMIC TURBULENCE STUDIES

of the AC components of the signals produced by the probes, one obtains results that are qualitatively indicated in Figure IV-3.

We note that as the probe B is moved downstream relative to the fixed probe A, two things happen. First, the time delay for maximum correlation increases with separation, as would be expected from the general flow of the liquid in the pipe. Second, the magnitude of the correlation diminishes and the width of the peak increases, giving information on the amplitude and coherence time of the turbulating eddies. This two probe cross-correlation technique for investigating turbulence and diffusion has applications in hydrodynamics, rocket exhaust studies, plasma physics, etc. It is probably the most important single tool available to investigators in these fields.

Another use of cross-correlation that is illustrative of yet another facet of this technique is in the characterization of linear systems. Lee and Wiesner[4]

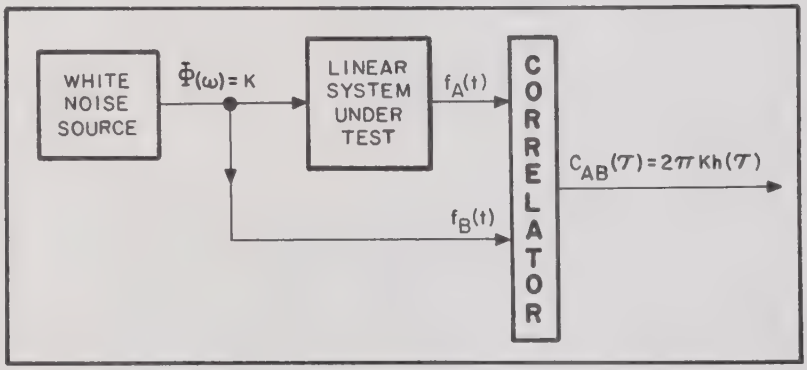


Figure IV-4. USING CROSS-CORRELATION TO DETERMINE SYSTEM IMPULSE RESPONSE

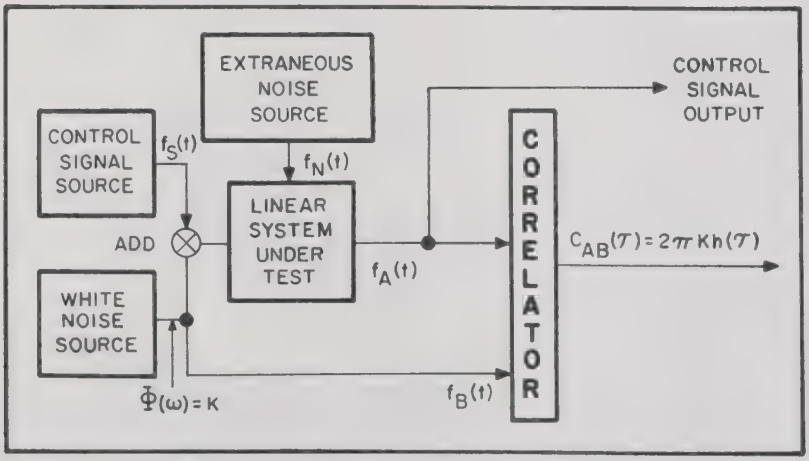


Figure IV-5. USING CROSS-CORRELATION TO RESPONSE-TEST AN OPERATING SYSTEM

[4]See page 345 of previous reference.

have pointed out that the unit impulse response of a linear system can be obtained by driving the system with broad-band white noise, and then determining the cross-correlation of this input with the system output, as illustrated in Figure IV-4. The cross-correlation function obtained is precisely the information sought, the unit impulse response of the system. The remarkable features of this method have important practical implications. Consider the effect which spurious noise might have on such an impulse response determination. Or, assume that the system is in constant use and is being driven by external signals as shown in Figure IV-5. It is possible in these cases to obtain the cross-correlation between the system output and the test white noise signal. Because there is no correlation between the test noise signal and the control signal or interfering noise, the presence of the two latter responses on the system output will in no way affect the cross-correlation obtained and the function will still be the impulse response, unperturbed by the extraneous signals. The immunity to internal system noise is also valuable as it allows the response to be obtained with very small exciting noise signals which will not interfere with the normal signals that the system is handling. The utility of such a technique is potentially very great, since the response of critical systems can be kept under constant surveillance, and adjustments made for optimum characteristics. Self-optimizing systems can, in fact, be constructed in this way. If feedback is introduced from a subsystem that evaluates the impulse response so that an optimum is maintained, we arrive at one form of a self-optimizing system.

Yet another application of cross-correlation with important practical consequences is in the extraction of signals of a known frequency from noise. In the physical sciences more often than not noise sets the limit on the sensitivity obtainable in a given experiment. If, as is often possible, the signals of interest can be made to appear at a known frequency and an additional clean reference signal obtained at the same frequency, then cross-correlation can be applied. The signal plus noise cross-correlated with the reference will yield a function that indicates the relative phase relationship between the signal and the reference. Also, the amplitude of the cross-correlogram will be the product of the reference amplitude and the signal amplitude, noise having been rejected. This powerful technique for recovering signals from noise is made use of in Lock-In Amplifiers,[5] which are extensively used in experimental research.

Important use of cross-correlation is also being made in the medical sciences. For example, Barlow et al[6] have demonstrated that significant changes occur in the auto- and cross-correlation functions obtained from electroencephalic signals of patients with brain tumors. Use has also been made of cross-correlation to localize that area of the brain that is responsible for uncontrollable muscular twitching in some diseases. Signals from strain gauges attached to twitching members cross-correlated with EEG signals from various parts of the brain permit the identification of the offending area.

---

[5] Lock-In Amplifiers for Signals Buried in Noise, R. D. Moore, "Electronics", June 8, 1963.

[6] See W. A. Rosenblith (ed.), Processing Neuroelectric Data, MIT Press, Cambridge, Mass.

SECTION V
THEORY AND CIRCUIT DESCRIPTION

5.1 INTRODUCTION

As stated previously, a Model 100 or a Model 101 Signal Correlator operates as a hybrid computer, utilizing both analog and digital techniques to solve the correlation function integral. These instruments can compute a correlation function in real time at 100 points simultaneously (the 100 points actually consisting of 100 consecutive one percent of computation time base intervals) by a parallel process of time shifting, multiplication, and averaging. To see more clearly how this is accomplished, briefly consider the "signal flow" through the instrument, referrring to the Signal Flow Diagram, page IX-3, as convenient.

The Channel A and Channel B Input Signals are handled differently. The Channel A Signal, after passing through the Coupling and Gain circuitry, is applied to a circuit called the Quantizer, the function of which is to convert an analog input into a pulse train of variable frequency and symmetry. The quantizer output in turn is sampled by a circuit which produces binary zeros or ones depending on whether the quantizer output is "up" or "down" at the instant a sample is taken. When the quantizer input is zero, its output is a symmetrical square wave and the number of sampler "one" outputs per unit time equals the number of "zeros". If the quantizer input is positive, the symmetry of the output pulse train shifts proportionally to the magnitude of the quantizer input. As a result, the probability that the sampler will detect an "up" becomes much greater than the probability that it will detect a "down", and the sampler generates a correspondingly greater number of "ones" per unit time than "zeros". Conversely, if the quantizer input is negative, its symmetry shifts oppositely, and the sampler generates more "zeros" per unit time than "ones". The Quantizer and Sampler work together to form a somewhat unconventional analog to digital converter, one based on probability and sampling rather than on direct analog to digital conversion.

What happens to the Channel A Signal after quantizing and sampling depends on whether the unit is a Model 100 or a Model 101. In the case of the Model 100, the "digitized" Channel A Signal is serially fed to the one hundred stage parallel-output Computer Shift Register. The signal is propagated through the register at the rate determined by the front panel Delay Range Switch, such that the time required to shift one "bit" through the register is the selected delay range. Note that the same oscillator drives both the Sampler and the Shift Register. Each stage of the Shift Register drives one input of a multiplier, the other input of which is driven by the Channel B Signal in analog form. The multipliers in turn drive RC averaging circuits (one for each multiplier). If correlation exists between the B Signal applied to any one multiplier and the converted and shifted A Signal which is applied to the other input of the same multiplier, the integrator capacitor, which serves as one element of the memory as well, becomes charged to the level of the correlation function at the point. This multiplication and averaging occurs simultaneously at all 100 "points", each representing a different value of computation delay. Provided the input signals are available for a period of five times the averaging time constant, the correlation function will be computed to within one percent of its final value and stored in the memory.

The Model 101 differs from the Model 100 in that an additional shift register can be inserted between the output of the Sampler and the input of the Computer Shift Register to obtain precomputation delay. Unlike the Computer Shift Register, the Precomputation Delay Register does not have parallel outputs, but is instead, a simple serial-in, serial-out type. Because it is driven at the same rate as the Computer Register, the amount of precomputation delay introduced depends on the "length" of the inserted register. If the Precomputation Period Switch is set to "0", the Precomputation Delay Register is completely out of the circuit, and the instrument is the same as a Model 100 Correlator. If the Precomputation Period Switch is set to "T", a 100 bit register is inserted between the Sampler and the Computer Shift Register, producing a precomputation delay equal to the selected Computation Period (Delay Range in the Model 100 and Computation Period in the Model 101 are completely equivalent). If the Precomputation Period Switch is set to "2T", the length of the inserted register is increased to 200 bits, with a corresponding increase in the precomputation delay to two times the selected Computation Period. Similarly, higher settings of the Precomputation Period Switch proportionally increase both the "length" of the inserted register and the duration of the precomputation delay (relative to the selected Computation Period). All circuits which follow the Precomputation Shift Register are exactly the same in the Model 101 as they are in the Model 100.

To read out a computed function, the memory is scanned by an extremely high impedance circuit, and the voltage to which each of the memory capacitors is charged is sequentially supplied to the output. Thus the signal available at the output connector consists of 100 consecutive pedestals. The height of each pedestal is the voltage to which the sampled memory capacitor is charged, and the width of each pedestal is the "dwell time" per memory stage, which in turn depends on the readout rate, Slow, Medium, or Fast. Additional circuitry provides the Time Base Outputs to facilitate readout with X-Y or strip-chart recorders at the slow and medium readout rates, or with an oscilloscope at the fast readout rate. When reading out at the fast readout rate, an additional "smoothing" filter can be inserted to provide a smooth continuous output function instead of a pedestaled function. Provision is also made for reading out, point-by-point, upon external command, this feature being particularly useful when the stored information is to be transferred into the memory of another computer.

In the following paragraphs, each of the above mentioned circuits will be treated in detail, not only with the object of indicating how they function, but also with the goal of clearly showing how each is related to the system as a whole.

5.2 INPUT CIRCUITRY

The input circuits of both signal channels are identical. Each consists of a front panel Input Jack, a Coupling Switch, and a step attenuator (Gain Selector Switch). For a detailed diagram of the input circuitry, refer to either the Quantizer Board Schematic, page IX-4, or the Channel B Amplifier Board Schematic, page page IX-7. Considering the input circuitry signal flow, any signal applied to the Input Connector is routed to the Coupling Switch. Whether or not the input signal will be applied to the input attenuator and hence to the input amplifiers, depends on the selected coupling mode. With

DC coupling, the signal is directly coupled. With AC coupling, it is coupled through a one microfarad capacitor, which, together with the input impedance, determines the low frequency cutoff point. In two of the remaining coupling modes, "GRD." and "CAL. 1V", the input signal is not applied to the input attenuator, but is instead "dead ended" at the Coupling Switch. The input to the attenuator, and hence to the input amplifiers, will be either ground or the one volt DC calibrate level, according to whether "GRD." or "CAL. 1V" has been selected. Finally, in the "A" and "B" positions, the signal applied to one input can be internally applied to both to facilitate auto-correlation operation. Note that both Gain Switches remain effective.

From the Coupling Switch the signal is applied to the input attenuator, which attenuates the signal as determined by the setting of the Gain Switch. Observing one of the detailed diagrams mentioned above, note that the attenuator consists of a series of "L" dividers, one for each position of the Gain Switch, except for the gain of five position in which no attenuation takes place. Note that the attenuation corresponding to each position of the Gain Switch is G/5, where G is the selected gain. The factor of five difference between the selected gain and the corresponding attentuation is compensated for by the net gain of the following circuits. That each selection of the attenuator will have a flat wide band frequency response is assured by the associated adjustable capacitor, which is adjusted to equalize the time constants of the two branches of each "L."

The signal at the output of the Channel A Input Attenuator is routed to the Quantizer Board, and that of Channel B is routed to the Channel B Amplifier Board. Each will be treated separately.

5.3 QUANTIZER BOARD

Most of the circuits located on the Quantizer Board are directly concerned with the quantizing action. Also located there are a few circuits, which, although essential to the quantizing action, are not directly involved in it. Observing the Block Diagram, page IX-2, note that the Channel A Signal is applied to the preamplifier, the "first" Quantizer Board circuit. Besides furnishing a gain of ten, the Preamplifier provides a low impedance output to the two circuits it drives, those being the Channel A Overload Detect Circuit and the Comparator at the input of the Quantizer proper. The Overload Detect Circuit warns the operator of quantizer overload by lighting the front panel Channel A Overload Lamp whenever the output of the preamplifier exceeds plus or minus four volts. The Comparator compares the signal from the preamplifier with that produced by the Sawtooth Generator and drives the next Quantizer Circuit, the Flip-flop. This circuit in turn drives two other circuits, the first being the Sawtooth Generator, which at any moment will be ramping positively or negatively depending on the state of the Flip-flop, and the second being the Buffer Amplifier, which supplies the pulse train (Flip-flop output) by way of a 15 nanosecond delay line to the sampler, which is located on another board.

As mentioned in the introduction, the function of the Quantizer is to generate a continuous pulse train, the symmetry of which is dependent on the amplitude of the Channel A Input Signal. To see how the Quantizer does this, it may be advantageous, while continuing to refer to page IX-2, to view the

Quantizer first of all as an operational amplifier, where the Comparator Amplifier is the input stage and the sawtooth generator is the output stage. Because the output of the amplifier is fed back to the inverting input and the preamplifier signal drives the non-inverting input, the "operational amplifier" acts as a unity follower for the Channel A Signal. However, it differs from conventional unity followers in that the output signal has a low amplitude sawtooth oscillation superimposed on it. To clearly see why this is so, consider the operation of the Quantizer when the preamplifier output is zero.

Assume initially that the flip-flop output is negative four volts. This assumption implies a further one, namely that the potential at the inverting input of the "operational amplifier" is also negative, though only slightly so. Because the output of the flip-flop is negative, the sawtooth generator will be ramping positively. Note, however, that as the ratio of the generator feedback resistor to its input resistor is one, the output voltage does not rise linearly, but instead rises according to the RC charging curve, where the instantaneous rate of change depends on how close the output voltage is to the magnitude of the applied level (4 V). This positive ramping continues until the level at the inverting input of the operational amplifier crosses over the zero level at the non-inverting input by an amount sufficient to make the flip-flop change state (typically ten millivolts). As soon as the flip-flop changes state, the generator sees plus four volts at its input and ramps negatively toward that level in response. Again the ramping continues until crossover by an amount sufficient to change the state of the flip-flop takes place. When this happens, the flip-flop changes state, marking completion of one cycle of the superimposed oscillation. So long as the input to the Quantizer is zero, a symmetrical sawtooth oscillation (amplitude typically 10 to 35 mV ptp) appears at the output of the sawtooth generator. This oscillation is referenced to ground because of the unity follower action of the quantizer as a whole. Likewise, the quantizer output, which is simply the flip-flop output, will be a symmetrical square wave.

The frequency of oscillation depends on several factors, among which are the time constant of the sawtooth generator, the gain of the Comparator Amplifier, and the hysteresis and output levels of the flip-flop. For all but the two fastest Delay Ranges, the zero level input oscillation frequency is 2 MHz. With the two fastest Delay Ranges, 0.2 ms and 0.1 ms, the frequency is increased to 3.5 and 5.0 MHz respectively to improve the step function response. The increase in oscillation frequency is accomplished by decreasing the capacitance around the sawtooth generator.

Now consider the quantizer operation if the preamplifier output shifts from zero to some positive level, say three volts. The flip-flop output which drives the sawtooth generator will be negative, and the sawtooth output will start rising toward plus four volts (the flip-flop output is minus four volts). It will continue rising until the three volt level is crossed over by an amount sufficient to change the state of the flip-flop. Just prior to cross-over the sawtooth output is at plus three volts and rising slowly (as determined by the RC curve) toward plus four volts. Just after cross-over it is still at plus three volts but charging rapidly toward minus four volts. Obviously, the negative going edge of the sawtooth will be much steeper and of shorter duration than the positive going edge. When the quantizer input

is positive, the sawtooth oscillation is still low level and it is still referended to the input level, three volts in this case. However, it is no longer symmetrical nor is it at the same frequency, both changes resulting from the nonlinearity of the RC charging curve. This assymmetry and frequency shift is reflected at the Quantizer Output; the flip-flop dwells much longer in one state than in the other and the period is longer as well. Should the quantizer input be negative, it follows that a corresponding but opposite symmetry shift will occur. Obviously, a continuously changing input function will appear at the quantizer output as a pulse train of continuously changing symmetry and frequency. Figure V-1 shows the relationship between the quantizer input voltage on one hand, and the sawtooth and flip-flop output symmetry on the other.

Note that the quantizer output waveform shown in Figure V-1 is "up" when the sawtooth is ramping positively, and "down" when the sawtooth is ramping negatively, in apparent contradiction to the preceding paragraphs. This is readily clarified when one realizes that whereas the differential flip-flop output is supplied to the Output Buffer and hence to the Sampler, only one of the flip-flop outputs drives the sawtooth generator. Whether the quantizer output should be shown "up" or "down" for a given ramping polarity depends purely on the choice of reference.

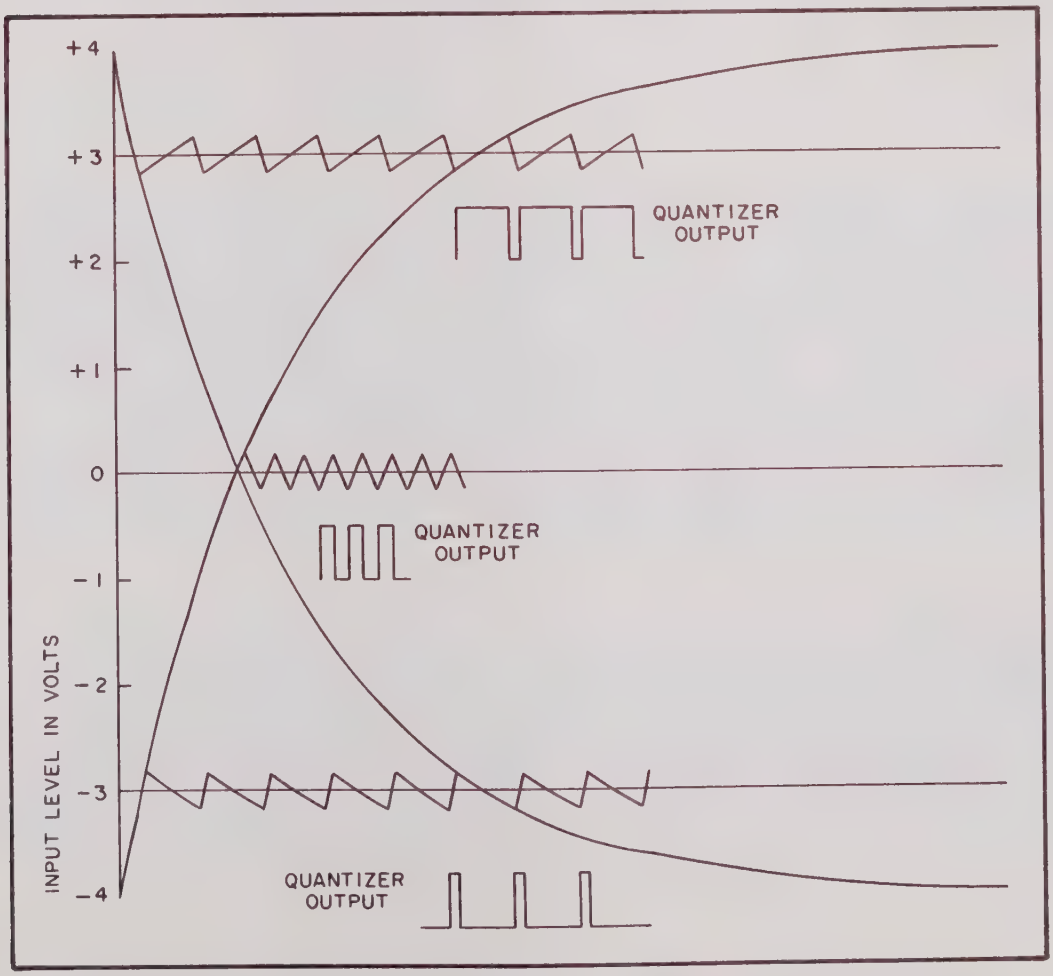


Figure V-1. QUANTIZER OUTPUT AS A FUNCTION OF CHANNEL A INPUT AND SAWTOOTH TIME CONSTANT

Figure V-2, a photograph of the Quantizer output with a sine wave Channel A input, is provided as a further illustration of the quantizing action.

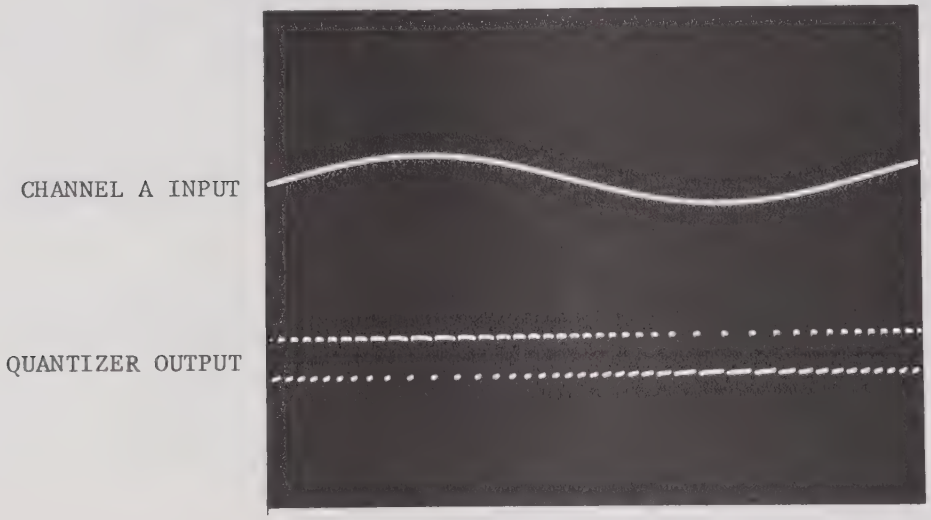


Figure V-2. QUANTIZER OUTPUT WITH SINE WAVE INPUT

PREAMPLIFIER

Observing the Quantizer Board Schematic, page IX-4, note that the Preamplifier comprises transistors Q603 through Q608 and their associated components. Considering the function of the components separately, Q603 is a constant current source for the input pair, Q604-Q605. Q606-Q607 constitute a second pair which provides additional gain. Finally, emitter follower Q608 provides a low impedance output to the Overload Detect Circuit and to the Quantizer. A feedback network, R620 and R614, establishes the preamplifier gain at ten, and the amplifier is connected as a non-inverting operational amplifier. Diodes D600 through D603 protect the circuit from damage induced by severe input overload. There are two adjustable components, the first being the capacitor C604, which is adjusted for a flat frequency response, and the second being the Zero Adjust Trimmer, R616, which is adjusted for zero at the preamplifier output when the input is zero.

OVERLOAD DETECTOR

Referring again to the schematic, note the Overload Detect Circuit (Q600 through Q602 and Q609 through Q611). The preamplifier output drives the phase splitter Q600-Q601, which in turn drives the full wave rectifier D604-D605. Transistors Q609 and Q610 form a comparator which compares the rectified signal with the DC level determined by the setting of the Overload Adjust Potentiometer, R632. Normally Q609 is off, as is Q611, the lamp drive transistor. When the rectified signal is sufficiently large, Q609 conducts, causing Q611 also to conduct. The overload indicator lamp lights and C609

discharges into D607. At the end of the overload period, C609, D606, and Q611 form a Miller Integrator which keeps the lamp energized for approximately one second longer than the overload interval, thereby assuring that even transient overloads will be noticed. Q602 is simply a constant current source for the pair, Q600-Q601.

QUANTIZER

The Preamplifier output stage, Q608, in addition to driving the Overload Detect Circuit, feeds one side of the Comparator (Q613-Q614). The other comparator input (base of Q614) is the output of the Sawtooth Generator (emitter of Q628). Q615 acts as a constant current source for the Comparator pair, and diodes D612-D613 limit the differential output of the Comparator to about six tenths of a volt. This voltage swing controls the following Flip-flop (Q616-Q617). Emitter followers Q620 and Q625 provide isolation between the Flip-flop output and the two following buffer amplifiers.

The first Buffer, Q618-Q619, supplies the variable symmetry pulse train (Quantizer Output) to the 15 nanosecond delay line which provides the necessary isolation between the Quantizer and Sampler Circuitry. The second Buffer, Q621-Q622, controls the Sawtooth Generator (Q626 through Q629), causing it to ramp positively or negatively depending on the state of the Flip-flop. Two additional circuits assure that the input to the Sawtooth Generator is limited to plus four volts or minus four volts. They are the constant current source, Q623, which limits the negative swing at the collectors of Q621 and Q622, and the constant voltage source Q624, which limits the positive swing. Note that the Quantizer Zero Adjustment, R671, establishes the Quantizer Output symmetry by allowing exact equalization of the positive and negative swings at the collectors of Q621 and Q622.

Transistors Q626 through Q629 constitute the Sawtooth Generator, essentially an operational amplifier with RC feedback between its output (emitter of Q628) and input (base of Q626). The input is referenced to ground (base return of Q627), and the closed loop gain of one is established by the ratio of the feedback resistor R676 to the input source impedance (R673). Transistor Q629 acts as a constant current source and supplies 1 mA. This current, flowing through resistor R680, provides the approximately seven volt difference in potential between the collector of Q626 and the base of the output emitter follower, Q628. Note that the feedback capacitance comprises C627, C625, and C626. On most ranges of delay, all three capacitors are in the circuit. The higher oscillation frequencies required on the two fastest ranges are achieved by successively decreasing the feedback capacitance by de-activating reed relays K603 and K604.

The feedback RC of the Sawtooth Generator gives the overall Quantizer a nonlinear frequency response. This is compensated by a network of equivalent time constant between the output of the Preamplifier and the input to the Comparator. Note that the time constant of this network is also controlled by reed-relays which "drop-out" capacitance on the two fastest Delay Ranges, thereby maintaining the time constants of the feedback and compensation networks equal. Note that ferrite beads are employed at several locations to prevent parasitic oscillations.

5.4 SAMPLER

The Quantizer Output is supplied to the Sampler by way of the already mentioned 15 nanosecond delay line. There it is periodically sampled for the duration of a ten nanosecond strobe pulse. As the sampling frequency is constant (100/T, where T is the selected Delay Range in seconds) for a given Delay Range, and absolutely independent of the Quantizer output frequency, the sampling is random; the number of sampler "one" outputs per unit time versus the number of sampler "zero" outputs per unit time depends only on the symmetry of the Quantizer output, which in turn depends on the Channel A input level. The 15 nanoseconds of delay between the Quantizer and the Sampler assure that a given ten nanosecond strobe pulse will not influence the quantizer state being sampled by that pulse.

Observing the Sampler Board Schematic, page IX-5, note that the Quantizer Output is supplied to the two common base amplifiers, Q900 and Q903, which in turn condition the sampler pair, Q901-Q902. The strobe pulse drives the emitters of the pair, and for its ten nanosecond duration will bias on one of these transistors, depending on the state of the Quantizer Output at the instant of the strobe pulse. For the duration of the strobe pulse, one transistor conducts and one of the two collector capacitors (C903-C904) is charged negatively. When the strobe pulse ends, the charged capacitor discharges through either R907 or R908, to produce a waveform with the characteristic RC curve trailing edge. Emitter followers Q905 and Q906 provide a low impedance drive to the following circuits.

The strobe pulse is derived from the T-Clock Pulse produced by an oscillator circuit on the "T-CLOCK" Board. This clock pulse is applied to the base of amplifier Q908, biasing it on for the duration of the pulse. The leading edge transient current is in turn coupled through C908 to another quiescently off amplifier Q907, which provides further shaping. Emitter follower Q904 provides a low impedance drive to the sample pair emitter circuit.

As in the Quantizer, ferrite beads are used extensively to suppress parasitic oscillations.

5.5 T-CLOCK

Referring to the T-Clock Board Schematic, page IX-6, observe that there are two circuits, the first being the oscillator (Q1000 through Q1006), and the second being the shaper (Q1007 through Q1009), which generates clock pulses to run the Shift Register(s) and Sampler.

The Clock Oscillator, in essence, is a triangular wave oscillator, the frequency of which is a function of the amplitude and slope of the triangular waveform. The slope depends on the charging rate of a capacitor. Changes in Delay Range change the value of the capacitor and/or the charging current, which is constant for a given Delay Range.

Considering the functions of the individual transistors, Q1000 is a constant current source, Q1001 and Q1002 are control transistors, Q1003 is a current inverter, Q1004 and Q1005 constitute a Schmitt Trigger which controls the direction of the charging current, and emitter follower Q1006 provides isola-

tion between the oscillator and the following shaper circuitry. Q1000, the constant current source, supplies current to the two control transistors Q1001 and Q1002, only one of which can conduct at a time. If Q1002 is conducting, the current supplied by Q1000 is routed through Q1002 to whichever capacitor is switched in by the Delay Range Switch, and the voltage on the capacitor rises linearly. If Q1002 is cut off, Q1001 conducts, biasing Q1003 on, and because R1003 and R1004 are equal and D1000 compensates the emitter base drop of Q1003, the current through Q1003 will equal that supplied by Q1000, though of opposite directions, and the voltage on the capacitor will descent linearly. Whether Q1001 or Q1002 conducts depends on the state of the Schmitt Trigger (Q1004-Q1005) because of the feedback from the collector of Q1005 to the base of Q1002.

Assume for the moment that positive ramping is taking place. For this to occur Q1002 must be conducting, and of the Schmitt Trigger transistors, Q1005 must be on and Q1004 off. Positive ramping continues until the voltage at the base of Q1004 is high enough to reverse the state of the Schmitt Trigger, that is, turn Q1004 on and Q1005 off. When Q1005 turns off, so does Q1002, turning Q1001 on and reversing the ramping polarity. Negative ramping continues until the cross-over voltage is reached, again reversing the Schmitt Trigger state and the ramping polarity. The restoration of positive ramping marks the completion of one cycle. Note that the feedback from the collector of Q1004 to the base of Q1005 separates the "turn-on" and "turn-off" threshold levels by several volts, thereby allowing the triangular waveform to be of sufficient amplitude to minimize drift effects.

The square wave signal at the collector of Q1004 is the oscillator output. Emitter follower Q1006 provides isolation. Trim-potentiometer R1008 determines the current supplied by Q1000 and so serves as the clock frequency calibrate adjustment. The remaining circuitry serves as a straightforward pulse shaper which produces the T-Clock Pulses from the positive going edges of the square waves at the emitter of Q1006. As mentioned previously, these Clock Pulses are routed to the Shift Register(s) and also to the Sampler Board, where further shaping takes place to form the strobe pulses.

5.6 B CHANNEL AMPLIFIER

Located on the Channel B Amplifier Board is the circuitry which amplifies the B Channel Signal prior to supplying it to the computer for comparison with the "quantized" Channel A Signal. Referring to the Channel B Amplifier Schematic, page IX-7, note that the Preamplifier and Overload Detect Circuits are the same on the B Amplifier as on the Quantizer. The quantizer circuit descriptions of those circuits apply to the corresponding B Amplifier Circuits as well. One small difference in the Preamplifier Circuits is worth noting, namely that the B Channel Amplifier gain is set at 7.5 instead of ten.

The remainder of the Channel B Amplifier constitutes an amplifier which acts as a level shifter and buffer between the preamplifier and the following computer circuits. Referring to the schematic, note that the amplifier comprises three separate circuits, a limiter (Q312 and Q313), the amplifier proper (Q314-Q315, and Q319-Q320) and a bias servo control circuit (Q316 through Q318).

Both of the limiter transistors are normally biased off. If the preamplifier output exceeds approximately +2.5 V, Q312 conducts and limits the positive voltage swing at that level. If the preamplifier output exceeds approximately -2.5 V, Q313 conducts and limits the negative swing.

The amplifier is basically an operational amplifier as illustrated in Figure V-3. The gain, as determined by the feedback resistors shown in Figure V-3, is unity from the preamplifier output to the "+B" output terminal, and minus unity from the preamplifier output to the "-B" output terminal.

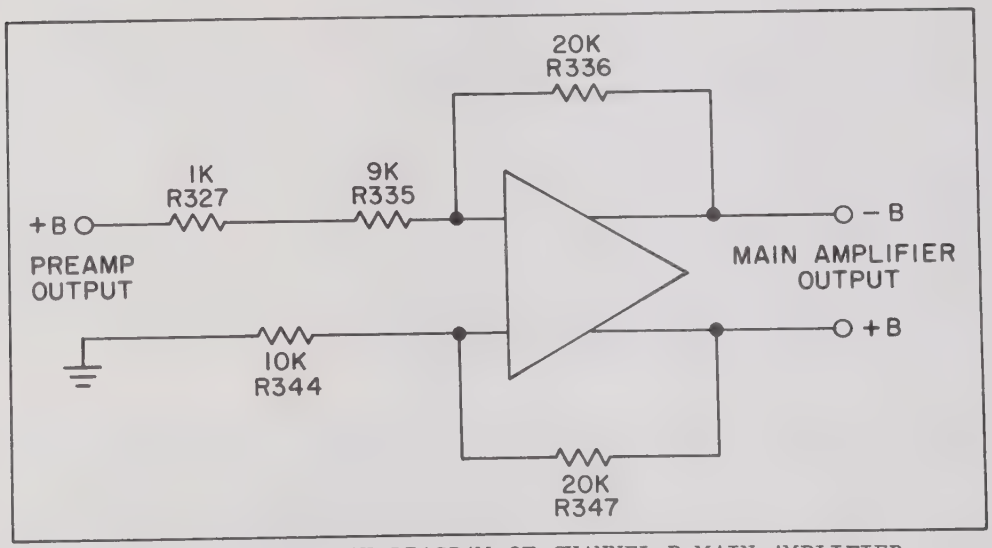


Figure V-3. BLOCK DIAGRAM OF CHANNEL B MAIN AMPLIFIER

The Bias Servo Control Circuit has a two-fold function. First of all, it establishes the amplifier output level at 7.8 volts (no input signal), and second, it maintains the common mode output balance, that is, it maintains the algebraic sum of the deviation from 7.8 volts of the "B" and "-B" terminals at zero. Observing the schematic, note that Q317 and Q318 form a differential amplifier. The reference for the amplifier is the 7.8 volt level at the base of Q317. This is compared with the common mode output level applied to the base of Q318. Any difference between the reference and common mode output level will result in a correction of the current supplied to the input pair by Q316, such as to re-establish the correct common mode level.

Note that the 7.8 volt "ERASE LEVEL" is simply the B Amplifier output reference level. There are two adjustments in the amplifier circuitry. The first is R337, which balances the limiters, and the second is R363, which allows a fine adjustment of the Bias Servo Circuit.

5.7 PRECOMPUTATION DELAY CIRCUITRY (Model 101 Only)

The Precomputation Delay Circuits are mounted on the Digital Delay Line Board, a hinged board attached to the bottom surface of the Mother Board beneath the chassis. Observing the Digital Delay Line Schematic, page IX-8, note that the Precomputation Delay Circuitry comprises four sections, those being: (1) the Clock Pulse Shaper, (2) the Input Driver, (3) the Output Schmitt Trigger, and, (4) a series of integrated circuit shift registers.

Of the four transistors in the Clock Pulse Shaper, Q1101 is a simple input inverter, Q1102 and Q1103 constitute a monostable, and Q1104 is an emitter follower which provides a low impedance drive to the shift registers. Note that the same clock pulse is applied to this circuit as is applied to the Sampler and to the Computer Shift Register; all three circuits operate in synchronism. As indicated by the waveforms shown on the schematic, the monostable (Q1102 and Q1103) produces a one microsecond wide pulse. However, when relay K1101 is de-energized, the time constant capacitance is reduced from 280 pF to 180 pF, which occurs when the shortest computation period (.1 microsecond) is selected. As a result of the reduced capacitance, the monostable output pulse duration is reduced from one microsecond to approximately a half microsecond.

As the clock pulse is supplied to the Clock Pulse Shaper, so the differential Sampler Output is applied to the Input Driver, which consists of a set-reset flip-flop (Q1105-Q1106) followed by a level shifter, Q1107. In essence, the Input Driver accepts the differential Sampler Output and in turn generates the single ended input required by the shift registers.

The output of the Input Driver is supplied to the first set of five 20-bit integrated circuit shift registers, SR1101 through SR1105, which provide the minimum 100 bit precomputation delay. Note that the shift registers are arranged in sets of five, each set of five providing an additional 100 bits of delay. How much delay is inserted at any time depends on the setting of the front panel Precomputation Period Switch, which determines which of the relays, K1102 through K1111, is energized. If the switch is set to "0", only K1102 will be energized, and the shift registers will be completely bypassed. If the switch is set to "T", K1103 will be the energized relay (only one at a time can be energized) and 100 bits of delay will be inserted. Similarly, successively higher settings will successively lengthen the precomputational delay in multiples of 100 bits. In units ordered with less than full precomputational delay capability, sockets are provided to facilitate adding additional sets of five 20-bit shift registers at a later date.

The remaining circuit on the Digital Delay Line Board, the Output Schmitt Trigger acts as a pulse shaper at the input to the Computer Shift Register. Essentially, the circuit accepts the single ended shift register output and provides the differential signal required by the following circuits. Briefly considering the function of the individual transistors which make up the circuit, emitter follower Q1108 provides a high input impedance, Q1111 is a constant current source for the drive transistors Q1109 and Q1113, and emitter follower Q1114 provides isolation between the Threshold Level potentiometer and Q1113. Q1110 and Q1112 constitute the actual cross-coupled

amplifier. Note that the output swing is from minus three volts (drop across diodes D1106 through D1109) to plus seven tenths of a volt (drop across D1117 and D1118).

5.8 COMPUTER BOARD CIRCUITRY

Located on the ten Computer Boards are the Computer Shift Register, the Multipliers, the Averagers, and the Gating and Readout circuits. The "digitized" Channel A Signal is serially fed to the Computer Shift Register, through which it is shifted at the clock rate to realize 100 incremental values of computation delay. Each of the 100 shift register stages drives a corresponding multiplier. At the same time, all multipliers receive the B Channel Amplifier Output. If there is any correlation between the Channel B Signal and the digitized and delayed Channel A Signal at any multiplier, the associated memory capacitor (averaging capacitor) gradually charges to a level proportional to the product of the two signals. Because there are 100 shift register stages, each with its associated multiplier and averager, the correlation waveform will be stored in the memory as 100 discrete voltage levels, or pedestals. By connecting these in sequence to a common bus through appropriate gating circuits, the correlation function is transferred to the output terminal. The functional relationship between the Shift Register, the Multipliers, the Averagers, and the Readout Gating Circuits, is clearly indicated on the Block Diagram, page IX-2, and on the Signal Flow Diagram, page IX-3.

Referring to the Computer Board Schematic, page IX-9, note the ten shift register stages (located in a "band" across the top of the schematic), each of which comprises four transistors and their associated components. Considering the first (upper left-hand corner) flip-flop stage as an example, Q822 and Q823 are the conventional cross-coupled amplifiers, and Q800 and Q801 are emitter followers in the cross-coupling circuits to improve switching speed. Capacitors C813 and C814 route the clock pulse simultaneously to both inputs (cathodes of D820 and D821), and diodes D800 and D801 limit the voltage swing at the collectors of Q822 and Q823 to 12 volts.

The circuit works as follows. The complementary Channel A output pulse train ("+A" and "-A") is applied to D820 and D821, biasing one of these diodes sufficiently close to conduction to allow the clock pulse to overcome the remaining bias and reach the base of either Q822 or Q823. If the transistor is conducting when the clock pulse is applied, it will turn off, changing the state of the flip-flop. If it is already off, no change takes place for that clock period. Because the output of one flip-flop is coupled to the next, and so on down the line, and all are driven by the clock pulse, any given sequence of states in the first stage (the statistical equivalent of the Channel A Signal) will be shifted along the register at the clock rate. The time required to shift one "bit" through the entire register will be the selected computation interval. It should be mentioned that the first shift register stage differs somewhat from the remaining 99 stages as indicated by notes "6" and "7" on the Computer Board Schematic.

Consider the remaining circuitry associated with the first shift register stage. Field effect transistors Q842 and Q843 form the multiplier, Q862 acts as a gate to isolate the multiplier from the averager during "Readout Only" and "Computation Gating" operation, R886 and C867 constitute the averaging circuit with C867 acting as the memory element as well, and Q872 is the read-

out gate, which, upon command, connects the level on the memory capacitor to the output bus. Note that except for the difference indicated in notes "6" and "7", each of the remaining shift register stages operates in conjunction with identical circuits.

The differential output of the B Channel Amplifier ("+B" and "-B" on the schematic) directly drives the drains of each multiplier pair. At the same time, the collectors of the associated shift register stage drive the gates of the multiplier transistors. The multiplier transistor driven from the "on" shift register transistor conducts. That driven from the "off" transistor does not. Gate Q862 is biased into conduction during computation so that the multiplier output, the common source of the Q842-Q843 pair, is applied to the averager.

The multiplier pair, in effect, is a full wave demodulator. If no "B" signal is present, the multiplier output will simply be the 7.8 volt B Channel output reference level, regardless of the A Channel Signal. If only non-synchronous "A" signals are present, the multiplier output averages to the same 7.8 volt level. If the "A" and "B" inputs to the multiplier contain the same in-phase frequency, synchronous rectification takes place, resulting in a more positive average output. Likewise, if the "A" and "B" inputs to the multiplier contain the same frequency but of opposing phase, the average output will be below the 7.8 volt level. In any case, the average output level relative to the 7.8 volt reference will always be proportional to the product of the "A" and "B" signals, and the averaging circuit capacitance (C867 in the example) will charge to that product level. Note that the capacitor is referenced to +8.2 volts, rather than to ground, to minimize leakage.

During computation, Q862 (and all other Computation Gate Transistors) will be biased on, connecting the multiplier output to the averager. During "Readout Only" operation, the transistor is biased off, inserting an effective open circuit between the multiplier and averager, and achieving the isolation necessary for the memory to "hold" the computed function after the signals being correlated are removed. Gated computation is also achieved by controlling the Computation Gate Transistors.

Q872 is the readout gate for the first memory capacitor. Note that each of the other memory capacitors has a corresponding memory gate and that all of these gates have a common output. During readout, each of these gates is biased on in sequence, making the memory contents sequentially available at the output for recording or other use.

During readout, the first of the ten Computer Boards is monitored first, beginning with capacitor C867. Q872 is turned on by pulling its gate to ground. On the first Computer Board, the gate of Q872 is driven from the "READ τ=0" logic circuitry located on the Programmer Board. The other 99 operate from a matrix of 99 simple Negative AND Gates (diodes D842 through D861). The matrix in turn is driven from a pair of ring counters located on the Counter Board. The two counters are designated "A" and "B", the "A" and "B" in no way referring to the two signal channels. According to the particular combination of "on" stages in the two counters, one diode gate may have both inputs down simultaneously, and the associated Readout Gate Transistor will sample the appropriate memory capacitor. The "A" Counter determines which of the boards will have the "on" gate and the "B" Counter determines which of

the gates on that board it will be.

Consider, for example, pedestal #14, the voltage level on the fourth capacitor of the second Computer Board. Its address is "A=2" (second board) and "B=4" (fourth stage on the board), and the readout command for the associated gate will be "2A·4B". All readout commands are negative, with an "off" level of +11 volts and an "on" level of 0 volts.

For the duration that a given readout gate is biased on, the common output bus is at the level of the associated pedestal. This level is monitored by the Output Buffer Amplifier (located on the Output Buffer Board), which provides isolation and level shifting before making the signal available at the output. Each of the 100 pedestals is monitored in like manner, the scanning rate being determined by the setting of the Readout Rate Switch. Note that the readout and computing functions are completely independent.

To see the interconnections between the Computer Boards and the associated circuits, refer to the Chassis Wiring Diagram, page IX-15 (Model 101, page IX-16). Note that the C(τ) Output Bus is common to pin 2 of each board, that the "Readout Only" or "Computation Inhibit" bus is common to pin 4 of each, and that the readout matrix wiring connects to pins 11 through 22, excluding pin 12, which is ground.

5.9 OUTPUT BUFFER BOARD

First among the circuits located on the Output Buffer Board is the high input impedance amplifier which, besides sampling the signal on the C(τ) bus, provides the level shift from the 7.8 volt reference on the C(τ) bus to the zero volt reference of the output circuits. This amplifier is followed by the Smoothing Filter, which is either "in" or "out" depending on the position of the rear panel Smoothing Switch. The last Signal Channel Circuit is the final amplifier which drives the C(τ) Output Jack, and, providing the Meter Switch is in one of the two output monitor positions, the front panel meter as well. Other circuits on the board provide erase and logic functions. The erase circuit will be considered with the amplifiers. The logic circuits, however, will be considered in the following discussion of the Readout Program.

Observing the Output Buffer Board Schematic, page IX-12, note that the signal on the C(τ) bus is applied to the amplifier comprising transistors Q201 through Q205 and their associated components. Considering their individual functions, Q203 is a constant current source which supplies current to the input pair, Q201-Q202, while pair Q204-Q205 furnishes additional open loop gain. The gain is established at three by feedback from the collector of Q205 to the base of Q202. An unusual feature of the amplifier is the level shift from the input reference of 7.8 volts to the output reference of zero volts. The necessary offset is provided by the voltage applied to the gate of Q202 from the C(τ) Zero Adjustment, R209. Note that a portion of the output signal is routed from the C(τ) Neutralize Adjustment, R211, through C204 to the input of the amplifier to neutralize the capacitance there.

The network between the output of the first amplifier and the input of the second has two functions. First, it allows calibration of the overall instrument gain by means of the rear panel Gain Calibrate Control. Second,

it contains the smoothing filter. Note that two capacitors are switched in or out by the rear panel Smoothing Switch. If the filter is "in" during fast readout, the effect will be to "smooth the steps". At the two slower readout rates the effect of the filter is negligible. Note that the 1000 pF capacitor is always in the circuit regardless of the position of the Smoothing Switch. Its purpose is to filter out switching transients.

The final amplifier (Q206 through Q211) is an operational amplifier with a feedback established gain of 1.2. Because of the similarity between this amplifier and the already discussed Quantizer Preamplifier, no detailed description is furnished.

Q200, the input shunt transistor switch, has a twofold function. First, it establishes the correlator output at zero whenever readout is not in progress, and second, it acts as the discharge path for erasing the memory contents. Whenever this transistor is biased on, it provides a low impedance path from the C(τ) bus to the 7.8 volt Erase Level from the B Channel Amplifier. As this corresponds to zero at the Buffer Amplifier Output, the correlator output will be at zero whenever Q200 is forward biased. If, at the same time, one of the memory capacitors is being sampled, that capacitor will be discharged through Q200 or erased. If scanning takes place, each capacitor is connected to the bus in sequence and discharged, and the entire memory contents are rapidly reduced to zero (7.8 volt reference level). From the schematic it is apparent that when the Readout Mode Switch is set to "ERASE", Q200 will be forward biased, and, providing the Readout Rate Switch is not set to "STOP", the memory contents will be erased. If the Readout Mode Switch is not set to "ERASE", Q200 will only be forward biased at specific times according to the "ZERO COMM." input, which is developed at the Programmer Board. During the interval between readout scans, no memory capacitor is sampled and the Zero Command to Q200 is at ground level, forward biasing the transistor and establishing the correlator output at zero. During the interval over which the memory contents are sampled, the Zero Command is at +12 volts, biasing Q200 off and allowing the stored information to appear at the output.

5.10 READOUT PROGRAM

If the amplitude of each pedestal is plotted against the A Channel delay time used to compute each pedestal, the resulting X-Y record is a correlogram. The vertical or C(τ) scale is in "volts squared", because each pedestal is produced by multiplying one input voltage by another (A Channel Signal by the B Channel Signal). The horizontal, or time base scale, is in units of time according to the selected computation interval, and is in no way a function of the plotting rate, that is, of the setting of the Readout Rate Switch. In the following discussion, mention is made of circuits located on several different boards. Consequently, the reader is advised to turn to the corresponding schematics as appropriate. As an aid in locating circuits, note that "100" series components are located on the Programmer Board (page IX-10), "700" series components are located on the Counter Board (page IX-11), and "200" series components are located on the Output Buffer Board (page IX-12).

The Readout Clock (Programmer Board Schematic, page IX-10) comprises transistors Q100, Q101, and Q103, along with their associated components. Q103 is

a Miller Ramp Generator which generates positive going linear ramps referenced to minus six volts. When a ramp goes slightly positive, the regenerative switch or hook, consisting of Q101 and Q100, turns on, discharging whichever ramping capacitor is in the circuit (a function of the selected readout rate) to reset the ramp. When the capacitor discharge current can no longer sustain conduction in Q101 and Q100, the two transistors turn off and another ramp begins. The ten volt output trigger pulse at the emitter of Q100 (the duration of which is the time required for the "hook" pair to discharge the capacitor) is applied to the Readout Rate Switch, and from there is routed to the Counter Board to drive the B Ring Counter. Note that when the Readout Rate Switch is set to "STOP", the pulse "dead ends" at the switch.

Referring to the Counter Board Schematic, page IX-11, note that the trigger pulses generated by the Readout Clock are applied to the base of Q725, which applies the advance command to the ten stage B Ring Counter (Q726, Q727, and Q757 through Q774). The output of this ring is a series of negative going pulses ("OFF"=+11 V, "ON"=0 V), each with a duration of one readout clock period. They are designated 1B, 2B, 3B, 4B, and so forth, according to the readout gate each controls. This ring counter cycles twelve times to produce one correlogram. As each cycle is completed, Q775 triggers Q700, which applies the advance command to the twelve stage A Ring Counter (Q701 through Q724). The output of this ring counter also consists of a series of negative going pulses similar to those produced by the B Counter, except that the duration of each A Output Pulse is ten readout clock periods. The A Pulses are designated 0A, 1A, --- 11A, and one cycle of the A Counter is required to produce one correlogram.

Recall for a moment the discussion of the Computer Boards, in which it was pointed out that each readout gate is controlled by a two way AND gate, with one input coming from the A Counter and the other from the B Counter. At any time one of the B Counter stages will be on. If, for example, "3B" is the on stage, the "3B" input to each of the ten Computer Boards will be biased on. However, there are two inputs to each readout gate, the second being the A Counter output. Each of the ten A Counter stages, "1A" through "10A", controls one Computer Board. Consequently, only a single readout gate on a single Computer Board can have both inputs on at one time, and only one memory capacitor can be sampled at a time. Recalling that the A Counter is a twelve stage counter, note that stages "0A" and "11A" drive none of the Computer Boards, with the result that no memory capacitor is sampled over the interval for which these two stages are on. These intervals are reserved for logic functions at the beginning and end of the readout program, as described under "X-Y RECORDERS", page III-20, and illustrated in Table V-1.

Referring again to the Counter Board Schematic, note that each ring counter produces a staircase output as well, this staircase being generated by successively shorting out the resistors of a divider as each ring stage turns on. These two staircases are added at the Programmer Board to produce the Time Base Output Staircase.

Table V-1 indicates the sampled pedestal and time base output level corresponding to any counter address (combination of the on "A" and "B" stages). observe that the "0A" and "11A" portion of the program is arranged to provide

ADDRESS	CORRELATOR OUTPUT	TIME BASE OUTPUT VOLTAGE
0A, 1B	Zero Volts	Zero Volts
0A, 2B	Pedestal 1	" "
0A, 3B	" "	" "
0A, 4B	" "	" "
0A, 5B	" "	" "
0A, 6B	" "	" "
0A, 7B	" "	" "
0A, 8B	" "	" "
0A, 9B	" "	" "
0A, 10B	" "	" "
1A, 1B	" "	+0.05 V
1A, 2B	" 2	+0.10 V
1A, 3B	" 3	+0.15 V
1A, 4B	" 4	+0.20 V
10A, 8B	Pedestal 98	+4.90 V
10A, 9B	" 99	+4.95 V
10A, 10B	" 100	+5.00 V
11A, 1B	Zero Volts	" "
11A, 2B	" "	" "
11A, 3B	" "	" "
11A, 4B	" "	" "
11A, 5B	" "	" "
11A, 6B	" "	" "
11A, 7B	" "	" "
11A, 8B	" "	" "
11A, 9B	" "	" "
11A, 10B	" "	" "
0A, 1B	" "	Zero Volts

Table V-1. READOUT PROGRAM SHOWING COUNTER ADDRESSES

a vertical trace at the beginning and at the end of the correlogram (assuming non-zero pedestal levels at these points), and a zero level horizontal retrace when the counters advance to 0A, 1B. Figure III-7, page III-22 shows such a recording.

Referring to the Readout Logic Diagram, page V-19, locate the AND gate consisting of D102 and D103 (Programmer Board). Assume that 0A*=0A (Operation Mode Switch not set to "READ τ=0"). For the duration of the first address (Table V-1) both 0A and 1B will be on, and the gate output will be at ground potential. Inverter Q106 drives Q110, which controls D118. D118 in turn turns on Q200 through D200, clamping the C(τ) bus to the 7.8 volt reference to produce zero at the output for the duration of the 0A, 1B address.

Note that when the Readout Mode Switch is in the Single Sweep position, Q106

also inhibits the Readout Clock by biasing the Miller Stage, Q103, into saturation, preventing any advance of the counters beyond the 0A, 1B address unless an "external" clock pulse is applied, either by pressing the front panel Single Sweep Trigger Pushbutton, or by applying a readout advance pulse to pin H of the rear panel Interface Connector.

Note that the 0A, 1B counter outputs are applied to the AND gate consisting of R234 and R235. The output of this gate is amplified by Q213 and Q214, which supplies the Trigger Pushbutton Switch and lights the Ready Light to indicate that the readout program is halted at the 0A, 1B address. Pressing the Trigger Pushbutton or applying an externally derived readout advance pulse causes the monostable (Q215-Q216) to generate a two millisecond pulse, which is fed through D220 to the counters. Providing the Readout Rate Switch is not set to "STOP", only one pulse is necessary to trigger the entire readout sequence. As soon as the counter advances past 0A, 1B, the Readout Clock is no longer inhibited, successive trigger pulses are produced, and the counter advances to complete the Readout Scan. Also, the Ready Light goes out and the Trigger Pushbutton is de-energized.

The situation is somewhat different with a combination of "SINGLE SWEEP" and "STOP". In this case the Trigger Pushbutton is supplied by way of D205. More important, application of a single trigger does not activate an entire readout scan sequence. Even though the Readout Clock oscillates as soon as the counter address advances beyond 0A, 1B, having the Readout Rate Switch in the "STOP" position prevents the clock output pulse train from being applied to the counters. As a result, each trigger pulse advances the counters one step only, and 120 triggers are required to complete an entire readout scan.

The following nine readout clock periods (addresses 0A, 2B through 0A, 10B) can be designated 0A·1B. Assuming again that the Operation Mode Switch is not set to "READ τ=0" so that 0A*=0A, the 0A·1B function is generated by Q105, D109, D111, and Q108. This function is routed through D120 to cause Q872 on the first Computer Board to read out the first pedestal. D116 and D119 generate the 1A·1B function, which acts through D121 to continue the readout of the first pedestal for one more clock period (1A, 1B). The remaining 99 pedestals are read out during the following 99 clock periods (1A, 2B through 10A, 10B).

During the final ten clock periods (11A, 1B through 11A, 10B), the 11A pulse is applied to Q200 by way of D117 and D200, again clamping the C(τ) bus to the 7.8 volt reference level to give zero at the correlator output. The next clock pulse restores the counters to their initial state (0A, 1B). Note that 120 clock pulses are required to advance the counters through one complete readout scan.

If the Operation Mode Switch is set to "READ τ=0", 0A*=1A, and the counters will not advance beyond 1A, 1B because the clock is inhibited by the 1A·1B function developed by D102, D103, and Q106. As a result, the first pedestal is continuously monitored and its level is available at the output.

To erase the entire memory contents, readout scanning must be in progress and Q200 must be biased on to discharge the memory capacitors in succession as

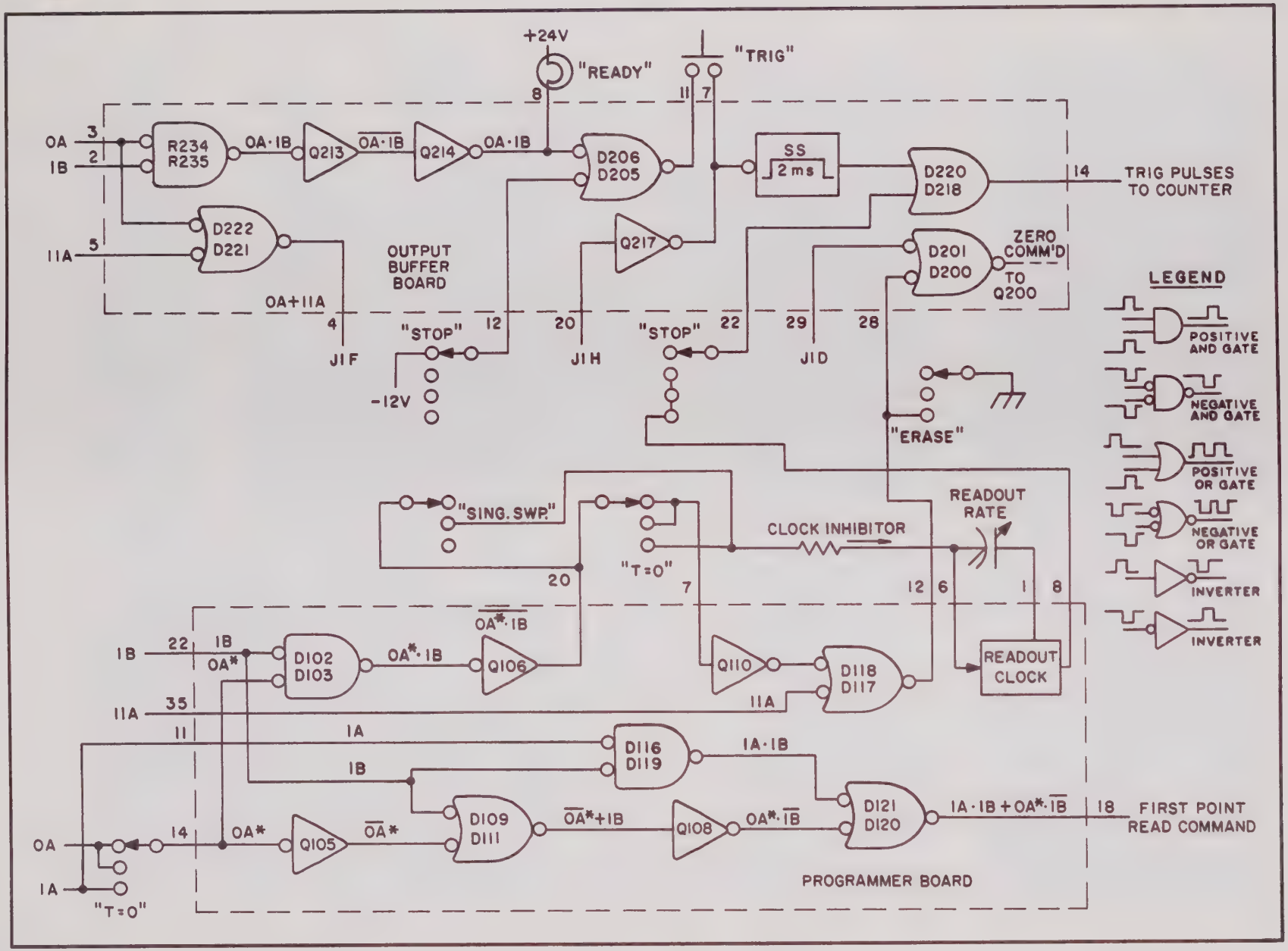


Figure V-4. READOUT LOGIC DIAGRAM.

each is connected to the C(τ) bus. Q200 can be biased on during the memory monitoring portion of the readout scan sequence either by setting the Operation Mode Switch to "ERASE", or by applying an appropriate level signal to pin D of the rear panel connector.

To complete the readout program discussion, note the as yet unmentioned OR gate consisting of diodes D222 and D221. The output of this gate is at plus one volt during 0A, +11 volts over the 1A through 10A interval, and ground again during 11A. This positive level coincides with the data portion of the readout program and constitutes the sync pulse which, regardless of the readout rate, appears at pin F of the Interface Connector, and, during fast readout only, at the Time Base Output Connector as well.

5.11 TIME BASE GENERATOR

Depending on the selected readout rate, two different outputs are available at the Time Base Output Connector. During fast readout, the positive trigger or gate pulse is available as described in the preceding paragraph. With the Readout Rate Switch set to "SLOW", "MED.", or "STOP", the output is a staircase function where the voltage level of any given "step" is the number of the pedestal being monitored, multiplied by 50 mV. For the 0A portion of the readout program, the output voltage is zero, and for the 11A portion it is +5 V. When the Operation Mode Switch is set to "READ τ=0", the Time Base Output is the level of the first staircase "step", or +50 mV.

The circuit which produces the staircase function is located on the Programmer Board. Referring to the Programmer Board Schematic, page IX-10, note that the two staircase functions generated at the Counter Board are applied to common base amplifiers Q111 and Q114. The "A" or "decade" counter switches smaller resistors than does the "B" or "units" counter, with the result that ten times more current is injected into Q111 "per step" than is injected into Q114. Because the two transistors have a common collector circuit, the injected currents add at the common collector to yield a 100 step voltage staircase which is proportional to the sum of both input staircase functions. As these functions are produced in the counters by successively shorting out a series of resistors as the counters advance, each step of the output staircase will correspond to the readout of a specific memory stage. As the staircase can be monitored with the front panel meter by setting the Meter/Monitor Switch to "TIME BASE", direct indication is available as to which of the 100 memory elements is being monitored at any time.

The following operational amplifier (Q112, Q113, Q115, and Q116) provides level shifting, inversion, and isolation. Its output, providing the front panel switches are appropriately set, is available at the panel meter and at the Time Base Output Connector. As this amplifier is similar to previously described amplifiers, no detailed description is furnished.

5.12 POWER SUPPLIES

With one exception, the regulated voltage levels used throughout the instrument are produced on the three Power Supply Boards. Power Supply #I supplies plus and minus twenty-four volts to the Quantizer Board. Power Supply #II supplies plus and minus twenty-four volts to all other boards with the ex-

ception of the ten Computer Boards. These two Power Supplies are identical and interchangeable. Power Supply #III supplies plus twenty-four, minus twelve, and plus 8.2 volts to the Computer Boards. In the case of a Model 101, this power supply furnishes plus twenty-four and minus twelve volts to the Digital Delay Line Board as well. Finally, the plus twelve volt clamping level used by the Computer Boards, and, in a Model 101, by the Digital Delay Line Board, is produced by returning the clamping diode current from all shift register stages through a zener diode (D13) located on a large heat sink. Some of the Power Supply #III transistors and rectifiers which handle high currents are also located on this heat sink, as indicated on the Power Supply #III Schematic Diagram, page IX-14, and on the Chassis Wiring Diagram, page IX-15. Because the regulator circuits on the Power Supply Boards are conventional in design, no detailed description is furnished.

The power supply system is illustrated in Figure V-5. Either 115 V or 230 V. 50-60 Hz, is routed through the thermal-overload cutout, the fuse, the Power Supply Switch, and the Line Voltage Selector Switch to the split primary windings of the Power Transformer. For 115 volt operation, the two primary windings are in parallel. For 230 volt operation, they are in series. There are three secondary windings, two of which supply rectifier bridges to produce the plus and minus thirty-one volt levels required by Power Supplies #I and #II. The third winding supplies two separate full wave rectifier circuits to produce the unregulated plus thirty-one and minus 17.5 volt levels required by Power Supply #III. Note that power to operate the fan is taken from one of the primary windings.

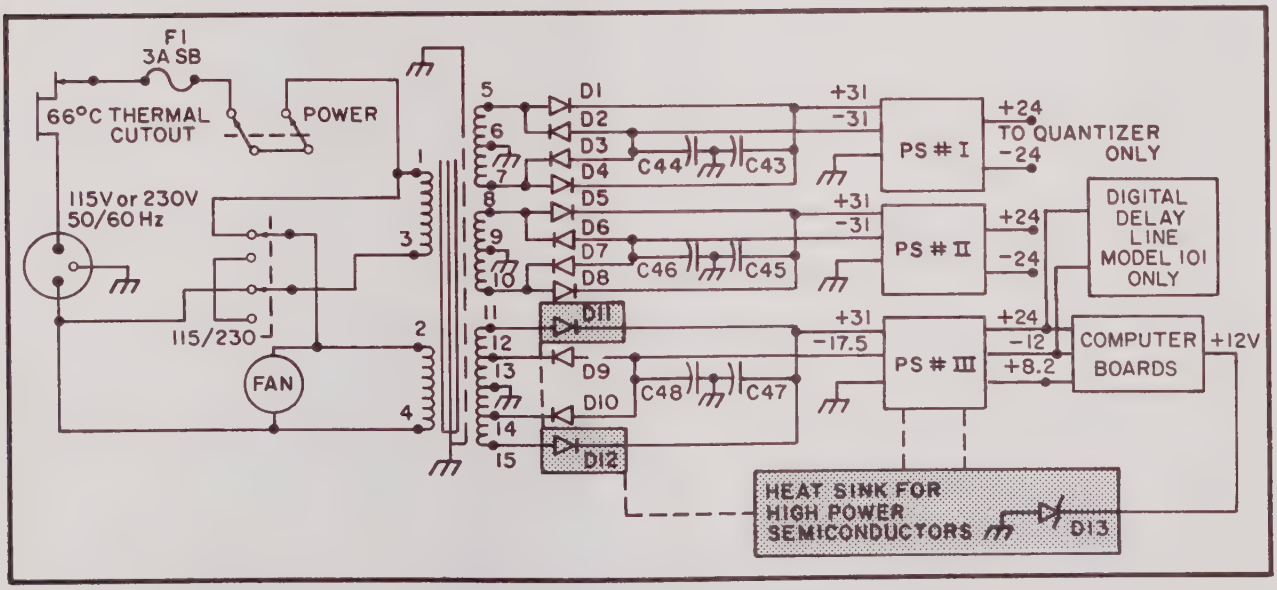


Figure V-5. BLOCK DIAGRAM OF THE POWER SUPPLY SYSTEM

SECTION VI
ALIGNMENT PROCEDURE

6.1 INTRODUCTION

PAR Correlators are stable, reliable instruments, and as such, should give long trouble-free service. To maintain the highest confidence in experimental measurements, however, the procedure outlined in this section of the manual should be performed twice yearly. A basic understanding of the instrument from an operator's viewpoint is a desirable prerequisite to performing a successful alignment.

The entire alignment should be performed in sequence. However, if time does not permit a complete alignment, any sub-assembly may be independently aligned, providing that any such partial alignment is followed by performing the zero adjustment as described under "ZERO ADJUSTMENTS" (page VI-12). The location of all Model 100 adjustments and test points is shown on Figure VI-1. In the case of a Model 101, it will be necessary to refer to the Digital Delay Line Layout Diagram, page IX-8, to locate the additional Model 101 adjustments. Appropriate nomenclature printed on the boards next to each adjustment provides further identification.

If any difficulty is encountered in performing the alignment and assistance is needed, contact the factory or an authorized representative. The PAR warranty appears in Section VIII of this manual and a list of authorized representatives appears at the end.

6.2 EQUIPMENT NEEDED

(1) Counter, capable of counting short pulses (100 nanoseconds) at repetition rates as high as 1 mHz, and capable of measuring a period of 60 ms to within one percent. Suggested instrument: HP type 3735 A or equivalent.

(2) Oscilloscope, having a rise time of 10 nanoseconds or faster, and a deflection factor of 50 mV/cm or better. Suggested instrument: TEKTRONIX type 543 B with a type 1A2 plug-in, or equivalent.

(3) Passive Oscilloscope Probe. Suggested type: TEKTRONIX series P6006 (010-0127-00) or equivalent.

(4) DC Voltmeter, 0.1% accurate at 24 V, input impedance one megohm or higher, capable of indicating zero volts plus or minus one millivolt. Suggested instrument: NLS type X-2 or equivalent.

(5) Square Wave Generator, capable of supplying a clean square wave having a rise time of 20 nanoseconds or better, and continuously adjustable over the range of 0.2 to 10 volts. Suggested instrument: HP 211 A or equivalent.

(6) Terminations appropriate to the above generator.

(7) Sine Wave Oscillator, capable of supplying a low distortion 1 kHz

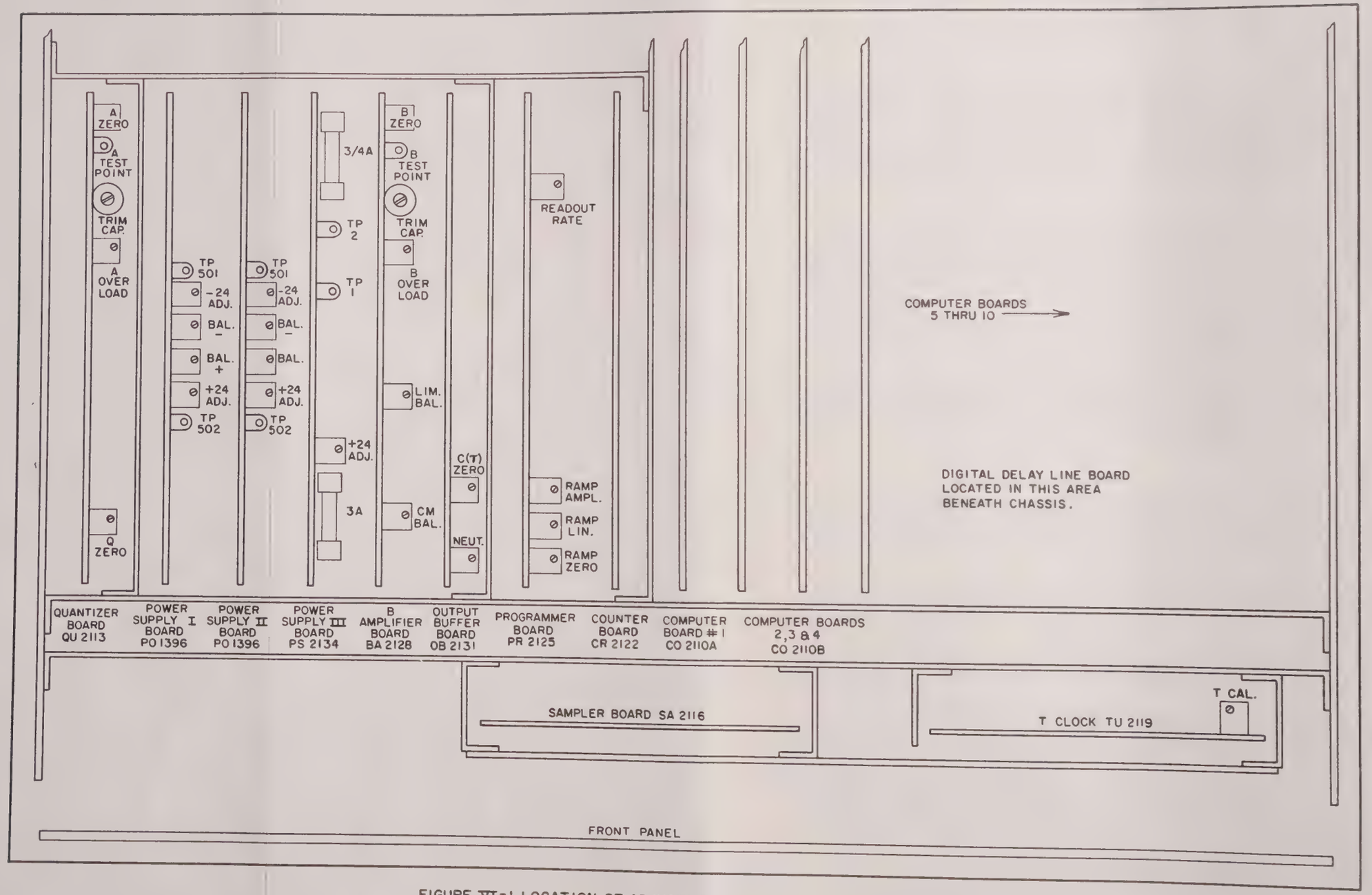


FIGURE VI-1. LOCATION OF ADJUSTMENTS AND TEST POINTS

signal continuously variable from 0.2 to 0.5 volts RMS.

(8) Extender Board, PAR #EB 1337.

6.3 PRELIMINARY STEPS

(1) Remove the two screws on the underside of the rear edge of the top cover. Slide the top cover free.

(2) Check, and if necessary, adjust the mechanical zero of the panel meter.

(3) If necessary, remove, clean, coat, and replace the air filter.

(4) Check the meter lamp. If it is discolored or burned out, replace it with a General Electric type 1813 or 1892.

(5) Check the Overload and Ready Lamps. If necessary, run through the initial checks (Section II) to set up conditions which will cause these lamps to come on. Replace any burned out lamp. Replacements are:

(a) Overload Lamps --- DIALCO #507-3917-1471-600 or #507-3918-1471-600

(b) Ready Lamp --- DIALCO #507-3917-1472-600 or #507-3918-1472-600.

(6) Replace the top cover and allow the instrument to warm-up for half an hour.

(7) Remove the top cover.

(8) Remove the two rear rubber feet and slide the bottom cover free.

(9) Proceed to align the instrument according to the following procedure. To gain free access to both the top and bottom, it may prove convenient to set the instrument on its side. Because the side panels slide free with the covers removed, they can easily be removed to prevent them from being scratched.

The temperature gradients developed with the covers off differ somewhat from the covers-on gradients. Consequently, after the alignment is completed, it is generally advisable to allow another half hour warm up with the covers on. Then recheck and, if necessary, retouch the Zero Adjustments (page VI-11).

6.4 POWER SUPPLIES I AND II (Board Type PO 1396)

(1) -24 ADJ.

(a) Monitor TP 501 of Power Supply Board #I with the DC voltmeter.

(b) Adjust the "-24 ADJ." Potentiometer until the meter indicates -24.0 volts.

(2) +24 ADJ.

(a) Monitor TP 502 of Power Supply Board #I with the DC voltmeter.

(b) Adjust the +24 ADJ." Potentiometer until the meter indicates +24.0 volts.

(3) Repeat steps one and two for Power Supply Board #II.

(4) If transistors have been replaced on either Power Supply Board #I or #II, make the remaining two adjustments on the affected board(s) as follows. If not, proceed directly to the alignment of Power Supply #III.

(a) Remove the Quantizer Board (QU 2113).

(b) If the power supply to be adjusted is Power Supply #I, remove it. If the power supply to be adjusted is Power Supply #II, or if both power supplies are to be adjusted, remove both boards.

(c) Short the bases of Q505 of the supply to be adjusted to each other. NOTE: Q505 is the pair of transistors cemented together and located below TP 501.

(d) Plug the board into the Power Supply #I socket.

(e) Monitor TP 501 with the DC voltmeter.

(f) Adjust "BAL -" for a meter indication of roughly -24 volts.

(g) Remove the short.

(h) Short the bases of Q510 to each other. NOTE: Q510 is the cemented pair located below TP 502.

(i) Monitor TP 502 with the DC voltmeter.

(j) Adjust "BAL +" for a meter indication of roughly +24 volts.

(k) Remove the short.

(l) Return the boards to their original positions.

(m) Check the voltages at TP 501 and TP 502 for -24.0 V and +24.0 V respectively. If necessary, repeat steps one and two for each board.

6.5 POWER SUPPLY III (Board Type PS 2134)

(1) +24 ADJ.

(a) Monitor Test Point #1 on Power Supply #III with the DC voltmeter.

(b) Adjust the associated potentiometer for a meter indication of +24.0 volts.

(2) Check that the voltage at Test Point #2 on Power Supply #III is -12 V, ±1 V.

6.6 PROGRAMMER (Board Type PR 2125)

(1) Ramp Zero Adjustment.

(a) Select "TIME BASE" with the Meter Switch.

(b) Select "COR. $0<\tau<T$" with the Operation Mode Switch.

(c) Select "FAST" with the Readout Rate Switch.

(d) Select "SINGLE SWEEP" with the Readout Mode Switch.

(e) Adjust "RAMP ZERO" for a panel meter indication of zero.

(2) Readout Rate Adjustment.

(a) Select "CONT." with the Readout Mode Switch.

(b) Connect the counter to the front panel "TIME BASE" Jack.

(c) Adjust "READOUT RATE" until the counter indicates a period of 60 ms.

(3) Ramp Linearity Adjustment.

(a) Connect the oscilloscope to programmer board pin 23, accessible from the bottom of the instrument.

(b) Adjust "RAMP LIN" until the observed sawtooth is free of discontinuities (Figure VI-2).

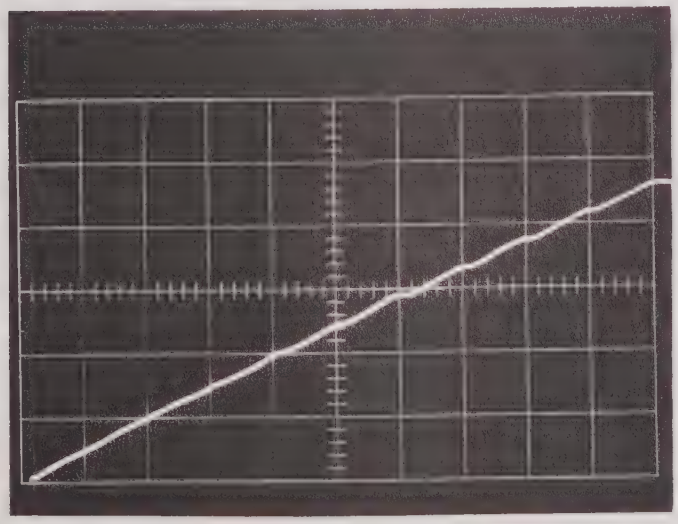


Figure VI-2. DISCONTINUITIES FROM IMPROPER ADJUSTMENT OF RAMP LINEARITY

(4) Ramp Amplitude and Ramp Zero Adjustments.

(a) Set the Meter Switch to "TIME BASE".

(b) Select "SLOW" with the Readout Rate Switch.

(c) Adjust "RAMP AMPL" until the panel meter indicates ramping from exactly zero to exactly full scale (readjust "RAMP ZERO" if necessary).

6.7 QUANTIZER (Board Type QU 2113)

(1) Preliminary Channel A Zero Adjustment.

(a) Select "5" with the Channel A Gain Switch.

(b) Select "GRD." with the Channel A Coupling Switch.

(c) Select "GRD." with the Channel B Coupling Switch.

(d) Connect the DC voltmeter to the quantizer board test point.

(e) Adjust "A ZERO" until the meter indicates zero, plus or minus 10 millivolts.

(2) Quantizer Trimmer Capacitor Adjustment.

(a) Select "DC" with the Channel A Coupling Switch.

(b) Apply a 0.2 V, 10 kHz square wave to the front panel "A INPUT" Jack.

(c) Connect the oscilloscope to the quantizer test point.

(d) Adjust the Quantizer Trimmer Capacitor for the best square wave.

(3) Preliminary Quantizer Zero Adjustment.

(a) Select "GRD." with the Channel A Coupling Switch.

(b) Connect the oscilloscope to quantizer board pin 22.

(c) Adjust "Q ZERO" until the observed square wave (approximately 2 mHz) is symmetrical.

(4) Channel A Overload Adjustment.

(a) Set the Channel A Coupling Switch to "DC".

(b) Model 100: Select ".1 mSEC." with the Delay Range Switch.

Model 101: Select ".1 mSEC." with the Computation Period Switch and set the Precomputation Period Switch to "0".

(c) Apply a 10 kHz square wave to the front panel "A INPUT" Jack.

(d) Monitor pin 22 of the Quantizer Board with the oscilloscope, which should be triggered from the square wave generator.

(e) Adjust the square wave generator amplitude until a pattern similar to that shown in Figure VI-3 is observed.

(f) Adjust "A OVERLOAD" until the Channel A Overload Indicator Lamp glows dimly.

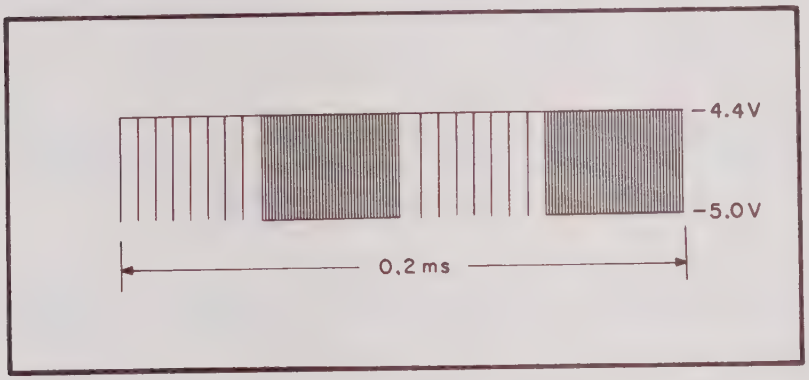


Figure VI-3. WAVEFORM PREREQUISITE TO MAKING THE A OVERLOAD ADJUSTMENT

(5) Correction of the value of capacitors C_z, C_y, and C_x.

It is unlikely that the values of these capacitors will ever have to be changed. However, if a change in value is indicated, be sure to proceed with care appropriate to sophisticated solid state circuitry. If the instrument is still in Warranty, contact the factory before considering any component changes. See paragraphs 7.1 through 7.3, Section VII. NOTE: The locations of these capacitors is indicated on the Quantizer Board parts layout diagram, page IX-4.

(a) Capacitor C_z has been selected such that the waveform obtained in step 4-(e) should appear more like Figure VI-3 than like Figure VI-4 or Figure VI-5. If a different value for C_z is indicated, a low temperature coefficient capacitor should be used.

(b) Except that the Delay Range Switch (Model 101 - Computation Period Switch) was set to ".2 mSEC.", capacitor C_y was selected in the same manner as C_z. The same temperature coefficient retriction applies.

(c) Except that the Delay Range Switch (Model 101 - Computation Period Switch) was set to ".5 mSEC.", capacitor C_x was selected in the same manner as C_z. The same temperature coefficient restriction applies.

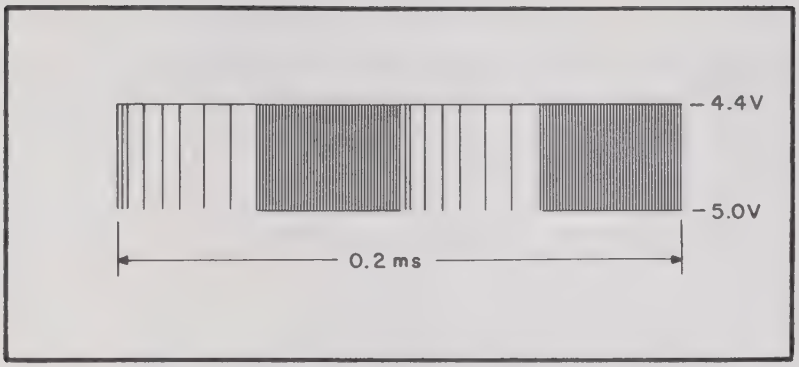


Figure VI-4. WAVEFORM OBSERVED WHEN CAPACITANCE OF C_z, C_y, OR C_x IS TOO LARGE.

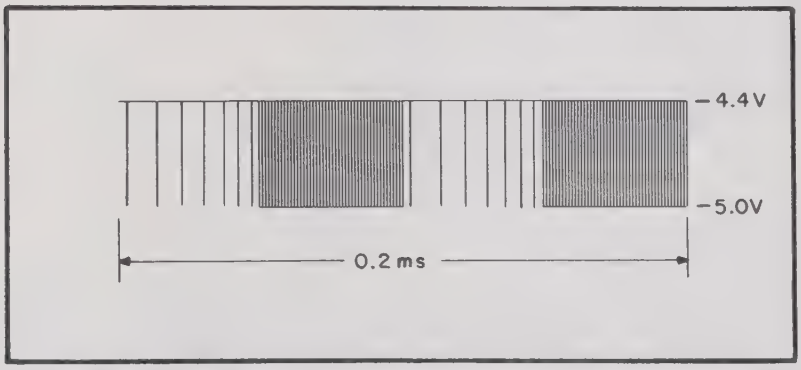


Figure VI-5. WAVEFORM OBSERVED WHEN CAPACITANCE OF C_z, C_y, OR C_x IS TOO SMALL

6.8 CHANNEL B AMPLIFIER BOARD (Board Type BA 2128)

(1) Preliminary Channel B Zero Adjustment.

(a) Select "GRD." with the Channel A Coupling Switch.

(b) Set the Channel B Gain Control to "5".

(c) Select "GRD." with the Channel B Coupling Switch.

(d) Connect the DC voltmeter to the Channel B Amplifier Test Point.

(e) Adjust "B ZERO" for a meter indication of zero volts, plus or minus 10 millivolts.

(2) Channel B Amplifier Trimmer Capacitor Adjustment.

(a) Set the Channel B Coupling Switch to "DC".

(b) Apply a 0.2 V, 10 kHz square wave to the front panel "B INPUT" Jack.

(c) Connect the oscilloscope to the B Amplifier Test Point.

(d) Adjust the B Amplifier Trimmer Capacitor for the best observed square wave.

(3) Limiter Balance and B Amplifier Overload Adjustments.

(a) Set the Channel B Coupling Switch to "AC".

(b) Connect the oscilloscope to pin 22 of the B Amplifier Board.

(c) Apply a 1 kHz sine wave to the front panel "B INPUT" Jack.

(d) Adjust the output amplitude of the generator until the oscilloscope indicates that slight limiting is taking place.

(e) Adjust "LIMITER BALANCE" until the observed clipping is symmetrical.

(f) Adjust "B OVERLOAD" until the Channel B Overload Indicator Lamp glows dimly.

(4) Common Mode Balance Adjustment.

(a) While continuing to apply the 1 kHz sine wave as directed in step 3, connect the oscilloscope to pin 23 of the B Amplifier Board.

(b) Adjust "CM BAL" for minimum observed ripple.

6.9 OUTPUT BUFFER (Board Type OB 2131)

Neutralization Adjustment

(a) Set the Smoothing Switch (rear panel) to "OFF".

(b) Select "COR. $0<\tau<T$" with the Operation Mode Switch.

(c) Model 100: Select "1 mSEC." with the Delay Range Switch.

Model 101: Select "1 mSEC." with the Computation Period Switch and set the Precomputation Period Switch to "0."

(d) Select "CAL. 1V" with both Coupling Switches.

(e) Select "1" with both Gain Switches.

(f) Set the Readout Mode Switch to "CONTINUOUS".

(g) Connect the oscilloscope to the $C(\tau)$ Output Jack. The oscilloscope sweep time should be 5 ms/cm and it should be triggered

from the positive slope of the pulse available at the Time Base Output when the "FAST" Readout Rate is in use.

(h) Adjust "NEUT" so that the first one percent of the display has the same amplitude as the remaining 99 percent. Be sure to allow for the integration time constant.

6.10 INPUT ATTENUATORS

Because the following procedure may weaken the wiring harness, it ought not to be performed unless it is certain that the frequency response of the attenuator has become degraded. One way of checking the response is to apply a 10 kHz square-wave input signal and observe the response with an oscilloscope at either "A TEST POINT" or "B TEST POINT", as appropriate. Adjust the amplitude of the input signal such that the amplitude of the observed waveform is one volt peak-to-peak. If a clean square wave is observed, no adjustment is required. If frequency response problems are noted, proceed as follows. Figure VI-6 identifies the individual trim-capacitors.

(1) Front Panel Removal.

(a) Remove the extrusion located above the front panel by first removing the four screws which hold it in place.

(b) Remove the four screws which secure the front panel.

(c) Lift the panel slightly upward. Then tip it forward and lay it on its face.

(2) Channel A Gain Switch Attenuator Adjustment.

(a) Connect a 10 kHz square wave to "A INPUT".

(b) Connect the oscilloscope to the Quantizer Board Test Point.

(c) Set the Channel A Coupling Switch to "DC".

(d) Set the Channel A Gain Switch to the range requiring adjustment.

(e) Adjust the generator output as desired, but keep it below the overload level.

(f) Adjust the trimmer capacitor corresponding to the selected gain range for the best observed square wave.

(3) Channel B Gain Switch Attenuator Adjustment.

(a) Connect a 10 kHz square wave to "B INPUT".

(b) Connect the oscilloscope to the B Amplifier Board Test Point.

(c) Set the Channel B Coupling Switch to "DC".

(d) Set the Channel B Gain Switch to the range requiring adjustment.

(e) Adjust the generator output level as desired, being careful not to overload the channel.

(f) Adjust the trimmer capacitor corresponding to the selected gain range for the best observed square wave.

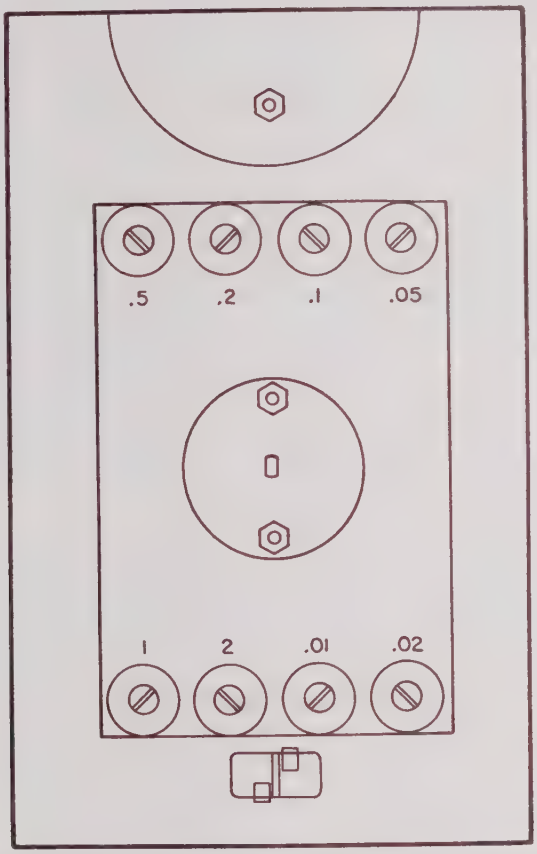


Figure VI-6. ATTENUATOR TRIMMER CAPACITORS (PANEL LOWERED)

6.11 COMPUTATION INTERVAL CALIBRATION ADJUSTMENT

(1) "T CAL" Adjustment.

(a) Model 100: Select "10 mSEC." with the Delay Range Switch.

Model 101: Select "10 mSEC." with the Computation Period Switch and "0" with the Precompuation Period Switch.

(b) Using as short a lead as is practical, connect the counter to pin 14 of the Sampler Board (SA 2116).

(c) Adjust "T CAL." (Circuit Board TU 2119) until the counter indicates a frequency of 10 kHz.

COMPUTATION INTERVAL (Delay Range or Computation Period)	FREQUENCY	TOLERANCE
10.0 seconds	10 Hz	±0.2 Hz
5.0 seconds	20 Hz	±0.4 Hz
2.0 seconds	50 Hz	±1 Hz
1.0 second	100 Hz	±1 Hz
0.5 second	200 Hz	±2 Hz
0.2 second	500 Hz	±5 Hz
0.1 second	1 kHz	±10 Hz
50 milliseconds	2 kHz	±20 Hz
20 milliseconds	5 kHz	±50 Hz
10 milliseconds	10 kHz	±100 Hz
5.0 milliseconds	20 kHz	±200 Hz
2.0 milliseconds	50 kHz	±1 kHz
1.0 millisecond	100 kHz	±2 kHz
0.5 millisecond	200 kHz	±4 kHz
0.2 millisecond	500 kHz	±10 kHz
0.1 millisecond	1 MHz	±20 kHz

Table VI-1. FREQUENCY AS A FUNCTION OF COMPUTATION INTERVAL (Model 100 - Delay Range, Model 101 - Computation Period)

(2) Computation Interval Tolerance Checks.

(a) Check all ranges of the Delay Range Switch (Model 101 - Computation Period Switch) by observing that the frequency indicated by the counter is as indicated in Table VI-1 for each position of the switch. It may be necessary to touch up the adjustment of "T CAL" to bring all Computation Intervals within tolerance.

6.12 ZERO ADJUSTMENTS (Always to be performed in sequence and as a group)

(1) Final "A ZERO" Adjustment (Quantizer Board, QU 2113).

(a) Select "GRD." with the Channel A Coupling Switch.

(b) Select "GRD." with the Channel B Coupling Switch.

(c) Set the gain of Channel A to "1".

(d) Set the gain of Channel B to "1".

(e) Model 100: Select "10 mSEC." with the Delay Range Switch.

Model 101: Select "10 mSEC." with the Computation Period Switch and set the Precomputation Period Switch to "0".

(f) Monitor the "A" test point (Quantizer Board) with the DC voltmeter and adjust "A ZERO" for an indication of zero.

(2) Output Buffer Zero, $C(\tau)$ Zero on Output Buffer Board, OB 2131.

(a) Set the Operation Mode Switch to "COR. $0<\tau<T$".

(b) Select "FAST" with the Readout Rate Switch.

(c) Select "SINGLE SWEEP" with the Readout Mode Switch.

(d) Monitor the $C(\tau)$ Output Connector with the meter and adjust "$C(\tau)$ ZERO" for a meter indication of zero.

(3) Final "B ZERO" Adjustment (B Amplifier Board, BA 2128).

(a) Set the Channel A Coupling Switch to "CAL. 1V".

(b) Set the Operation Mode Switch to "READ $\tau=0$".

(c) While continuing to monitor the $C(\tau)$ Output Jack with the voltmeter, adjust "B ZERO" for a meter indication of zero. Be sure to allow sufficient time for the output to fully respond (standard time constant is 20 seconds) each time the potentiometer setting is changed.

(4) Final "Q ZERO" Adjustment (Quantizer Board, QU 2113).

(a) Select "GRD." with the Channel A Coupling Switch.

(b) Select "CAL. 1V" with the Channel B Coupling Switch.

(c) Adjust "Q ZERO" for zero at the $C(\tau)$ Output Jack, taking the response time into account.

(5) Clock Pulse Width Adjustment (Model 101 only).

(a) Set the Precomputation Period Switch fully clockwise.

(b) Set the Computation Period Switch to ".1 mSEC."

(c) Locate the Digital Delay Line Board, which is located beneath the chassis. Note that the board is hinged at one end and that it can swing away from the chassis after loosening two screws. Proceed to loosen the two screws and swing the Digital Delay Line Board out far enough to gain access to the two adjustments located on that board. Refer to the Digital Delay Line Layout Diagram, page IX-8, to identify the two adjustments.

(d) Determine which of the two 3/4 turn trimmer potentiometers located on the Digital Delay Line Board is the Clock Pulse Width Adjustment.

(e) While continuing to monitor the $C(\tau)$ output, begin turning the Pulse Width Trimmer slowly clockwise, taking care not to force the adjustment beyond the stop. At some point during the clock-

wise adjustment, the C(τ) output may begin to shift negatively or positively. By rotating the control slightly back and forth, note carefully where this point is. If no C(τ) shift takes place, assume the "point" to be at the end of the clockwise range of adjustment. Then turn the control counter-clockwise. After passing through the range of normal operation (approximately zero C(τ) output), another point may be reached where a C(τ) shift takes place. Again note carefully where the point is in terms of adjustment rotation. If no "break" point is noted, assume it is at the end of the counter-clockwise range of adjustment. Finally, having precisely determined both "break" points, set the control midway between them, i.e., in the middle of the range of "normal" operation. If normal operation cannot be obtained, make the adjustment with the Computation Period Switch set to ".2 mSEC." As indicated in the specifications, precomputation operation is not guaranteed with a computation period of ".1 mSEC."

(6) Threshold Adjustment (Model 101 only)

(a) While continuing to monitor the C(τ) output, begin alternately switching the Precomputation Period Switch back and forth between "0" and "T."

(b) Allow the switch to dwell in each position for at least one time constant (nominally 20 seconds). Observe that a slight shift in C(τ) may accompany each change in switch position. If such a shift is observed, adjust the Threshold Control (the other Digital Delay Line Board Adjustment) as necessary to eliminate the shift.

(c) Secure the Digital Delay Line Board in its proper position.

6.13 GAIN ADJUSTMENT (Rear Panel)

(1) Select "CAL. 1V" with both Coupling Switches.

(2) Select "1" with both Gain Switches.

(3) Set the Readout Rate and Readout Mode Switches to "FAST" and "CONT." respectively.

(4) Set the Operation Mode Switch to "READ τ=0".

(5) Connect the DC voltmeter to the C(τ) Output Jack.

(6) After allowing time for the output indication to stabilize (five time constants), adjust the rear panel "GAIN" Control for a meter indication of one volt. This step completes the alignment. Remove the test equipment and replace the covers.

SECTION VII
TROUBLESHOOTING GUIDE

7.1 INTRODUCTION

Featuring conservative design, quality components, and solid state circuitry throughout, PAR Signal Correlators are precision, highly reliable instruments, and as such, should provide long trouble-free service. Component deterioration or failure, however, could cause an instrument to no longer "meet specs", or even to become inoperative. Should this occur, a partial or complete performance of the alignment procedure (Section VI) will generally restore proper operation. In those cases where the malfunction is a result of component failure, aligning the instrument will, of course, prove to be impossible.

By following the procedures outlined in the following pages, one should have little difficulty in isolating the problem to a single circuit board. Once the board is located (or before), the user should contact PAR for advice on the relative merits of repairing the board himself as opposed to returning it to PAR for repair. Checking while referring to Section V ("THEORY AND CIRCUIT DESCRIPTION"), will probably result in locating and replacing the faulty component. In any case, if the instrument is still in warranty (Section VIII), it is particularly important that PAR be contacted prior to attempting a field repair. Failure to do so could invalidate the Warranty.

As an aid to troubleshooting, voltage and waveform information appears on the schematics (Section IX) at critical points. Although the oscilloscope specified below is fast enough for general troubleshooting, it is not capable of displaying some of the faster waveforms indicated; a sampling unit with a very low capacitance probe is required.

7.2 WARNING

The field effect transistors used on the Computer Boards are easily damaged by static discharge. Consequently, precautions MUST be taken to avoid such discharge if any of these boards are removed. Suitable precautions include:

(1) Unplugging the line cord prior to handling the Computer Boards.

(2) Shorting out the group of pins at each end of a Computer Board whenever one is removed. Ideal shorting bars are easily constructed from 1/64" brass shim-stock. Two pieces, 3/8" x 2½" are required for each board. To install a shorting bar, simply push it into the pin slots.

(3) Wrapping Computer Boards in aluminum foil if they are to be stored outside the instrument. Under no circumstances should a Computer Board be wrapped in plastic or placed in a plastic bag.

(4) Working on a conducting, grounded workbench.

(5) Continuously touching ground for the entire period the Computer Boards are being handled.

(6) Continuously grounding the tip of a soldering iron being used to work on a Computer Board.

NOTE: In the case of the Model 101, similar precautions must also be taken in handling the integrated-circuit modules which plug into sockets on the Digital Delay Line Board.

7.3 SOLDERING TECHNIQUES FOR PRINTED CIRCUIT WORK

If any components are removed from the printed circuit boards for inspection or replacement, be especially careful not to damage the print. To remove components "cleanly" requires considerable care. The recommended method is "wicking." The following procedure is suitable for removing components from single sided boards (boards having print on one side only).

(1) Dip a few inches length of stranded wire (shielding braid is ideal) into some rosin base soldering flux, and then place the wire on top of the joint to be unsoldered, allowing some of the flux to flow over the joint. NOTE: Under no circumstances use an acid base flux.

(2) As shown in Figure VII-1, place a hot soldering iron (no larger than 40 watts) on top of the stranded wire directly above the joint to be unsoldered. Within a few seconds, most of the solder in the joint will flow quickly up the "wick", leaving the joint area free of solder.

(3) Lift the soldering iron and remove the "wick" before it freezes to the joint. Cut off the "filled" end of the wick (generally about 1/2 inch should be removed).

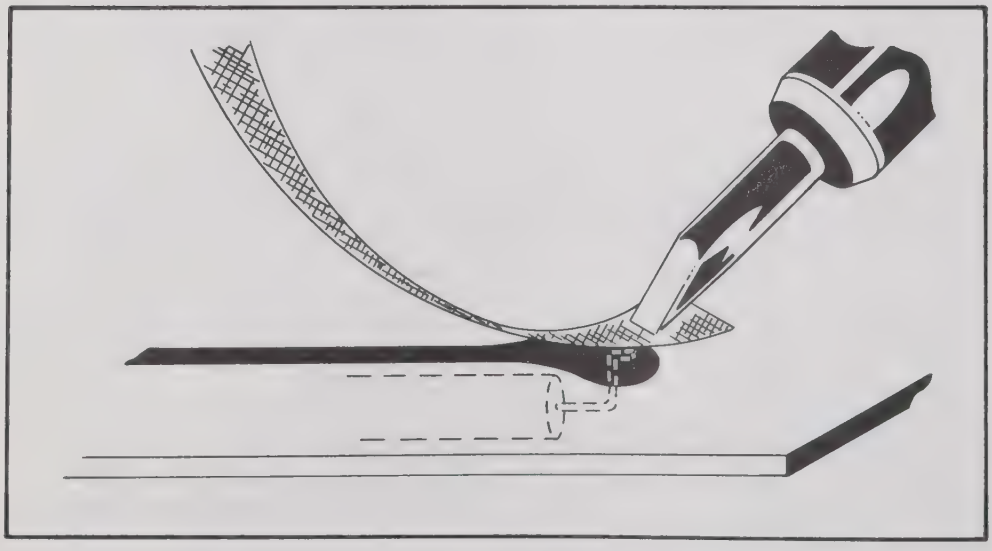


Figure VII-1. SOLDER REMOVAL BY WICKING

(4) Inspect the joint. If any solder remains, repeat steps "(1)" through "(3)" to remove any remaining solder. It should then be very easy to straighten the component lead so that the component can be removed after repeating the procedure with the other lead(s).

In returning the component or its replacement to the board, make sure that the leads are bent on the proper centers, and that they don't "angle in" or "angle out". If they do not pass freely through the centers of the holes, they may catch the edge of the print and lift it. Cut off the excess lead length and bend the leads over. Solder them with a hot iron (NO LARGER THAN 40 WATTS), using a good grade of rosin core 60/40 solder. Be sure to apply heat no longer than necessary to achieve a good joint (usually a few seconds with a properly tinned hot iron). After soldering, clean the board with flux remover (Alpha 653 or equivalent). NOTE: No harm will result from leaving the flux on the board other than to degrade the appearance of the board.

Most of the Model 100 and Model 101 printed circuit boards are two sided boards (boards having print on both sides). Many of the mounting holes on these two sided boards are plated-through holes, which usually fill with solder when the components are mounted. As a result, somewhat different techniques must be utilized in removing and replacing components. A suitable procedure follows.

(1) Proceed as in the case of "normal" holes up to where wicking is completed and the leads straightened.

(2) Grasp the lead to be removed with long nose pliers on the component side of the board (the board should be clamped in place). Touch the soldering iron tip to the straightened lead while pulling (gently) the component away from the board with the pliers. When the solder in the holes flows (usually in a few seconds), the component can be pulled from the board at that end. Repeat for the other end and remove the component.

(3) Removing transistors and trim-potentiometers pose special problems because these components will not move with just one lead "freed". To remove such components, one must move the soldering iron tip from one lead to the next while pulling gently directly away from the board. By applying the iron to each lead for a second or two and then advancing to the next lead, all should become evenly heated, and the solder will flow in all holes at about the same time, allowing the component to be easily pulled straight away from the board.

As removing components from plated-through holes is a special problem, so is replacing components, because the holes must first be cleared of the solder which fills them. The most satisfactory technique is to melt the solder by touching the soldering iron tip to the "pad" for a few seconds, followed by quickly rapping the board, once, against the bench. The solder will fly out, leaving a clear hole. In applying this technique, it is important to move quickly, because the solder will usually freeze within a second or two after removing the iron. Do not attempt to extend the time the solder is molten by applying heat longer than necessary as this may cause the print to become detached from the board. Also, there is no point in making more than one tap per heating. By the time the second tap is made, the solder will have

frozen. After clearing the solder from the holes, inspect the board closely to be sure, very sure, that no solder has splashed onto the board and shorted out adjacent ribbons. If such a solder splash is noted, remove it by wicking.

Using these techniques, no damage to the board or print will take place, and after completion of the job, the board should be indistinguishable from one which is "fresh from the factory".

7.4 EQUIPMENT NEEDED

(1) General purpose oscilloscope such as the TEKTRONIX type 543 with a type CA plug in.

(2) DC voltmeter, 0.1% accurate, such as the NLS type X-2.

(3) Extender Boards --- Although the extender boards are not generally required to isolate a problem to an individual board, they are required to isolate the problem to an individual circuit or component. Five different types are required. All are available from PAR. The part number of each, along with the circuit board(s) each "fits", follows.

(a) EB 1337, All Power Supplies, the Quantizer, and the B Amplifier

(b) EB 2573, Output Buffer

(c) EB 2575, Programmer and Counter

(d) EB 2577, Computer

(e) EB 2579, Sampler and T-Clock

7.5 PRELIMINARY STEPS

(1) Disconnect all associated equipment from the Correlator.

(2) Disconnect the AC line cord.

(3) Remove the two screws on the underside of the rear edge of the top cover. Slide the top cover off.

(4) Remove the two rear rubber feet and slide the bottom cover off.

(5) Connect a jumper across the thermostat located on the heat sink assembly near the power transformer. Refer to the Chassis Wiring Diagram, page IX-15, to determine points convenient for jumping.

(6) Reconnect the line cord and turn the power on.

7.6 POWER SUPPLIES

(1) Because a malfunctioning power supply can cause any number of problems, the first step in isolating a trouble is to ascertain that the

various power supply and reference levels are within tolerance. The supplies, references, and circuits served by each are:

(a) Power Supply I supplies plus and minus 24 V to the Quantizer.

(b) Power Supply II supplies plus and minus 24 V to all other circuits except the Computer Section.

(c) Power Supplies I and II are interchangeable.

(d) Power Supply III supplies plus 24 V at up to three amperes to the Computer Section, minus 12 V for various uses, and plus 8.2 V to the Memory Capacitor Common. In the case of the Model 101, this power supply furnishes +24 V and -12 V to the Digital Delay Line Board.

(e) The Computer Section supplies current for the plus 12 V power bus which is regulated by a high current zener diode on the heat sink assembly. This bus supplies the Counter, Logic Circuits, and the Meter Lamp.

(f) The B Amplifier provides the plus 7.8 V level for the Erase and $C(\tau)$ reference.

(2) The following table indicates the power supply and reference levels and tolerances. Refer to Figure VI-1, page VI-2, for the location of the indicated test points. As these supplies are somewhat interdependent, the most independent ones are listed first.

SUPPLY MEASURED	WHERE	VOLTAGE
Power Supply I	TP 501	-24 ±0.1 V
Power Supply I	TP 502	+24 ±0.1 V
Power Supply II	TP 501	-24 ±0.1 V
Power Supply II	TP 502	+24 ±0.1 V
Power Supply III	TP 2	-12 ±0.25 V
Power Supply III	TP 1	+24 ±0.25 V
Power Supply III	Pin 14	+8.2 ±1 V
Computer (any)	Pin 31	+12 ±1 V
Channel B Amplifier	Pin 23	+7.8 ±0.25 V

7.7 ISOLATING THE MALFUNCTION

(1) Set the Correlator Controls as follows:

Channel A GAIN	1
Channel A COUPLING	GRD.
Channel B GAIN	1
Channel B COUPLING	CAL. 1V
Model 100:	
Delay Range	.1 mSEC.
Model 101:	
Computation Period	.1 mSEC.
Precomputation Period	0

Operation Mode Switch ---------- COR. $0<\tau<T$
Readout Rate Switch ---------- FAST
Readout Mode Switch ---------- CONT.
Smoothing Switch (rear panel) ---------- OFF

(2) Connect the oscilloscope to the $C(\tau)$ Output Connector. The oscilloscope should be DC coupled and the sensitivity should be 0.5 V/cm. Trigger from the Correlator Time Base Output Pulse (plus one to plus twelve volts). Set the oscilloscope sweep time at 5 ms/cm.

(3) Observe the oscilloscope trace. A normal indication would be a straight horizontal line referenced to zero volts. If there is a Correlator malfunction, in all likelihood a different pattern will be observed. If the pattern shows a random distribution of high level positive or negative pedestals, or if there is no pulse available at the Time Base Output Connector, the problem is probably not in the Computer Section. If the pattern shows a single channel discontinuity, or is zero for a portion of the trace and high positive or high negative for the remainder, the problem is probably in the Computer Section.

7.8 COMPUTER SECTION

Each of the ten Computer Boards generates one tenth of the correlogram, that is, each Computer Board computes the amplitude of ten pedestals, each pedestal having a duration of 0.5 ms at the fast readout rate. The Computer Board on the far left of the Computer Compartment computes the first 5 ms of the correlogram, that to the right of the first computes the second 5 ms, and so on up to the last Computer Board, which computes the final 5 ms. As a result, the Computer Board responsible for an observed discontinuity (Figure VII-2 shows two such discontinuities) can easily be determined by the timing of the discontinuity. If there is any doubt, the suspected board (other than the first) can be interchanged with any of the remaining Computer Boards.

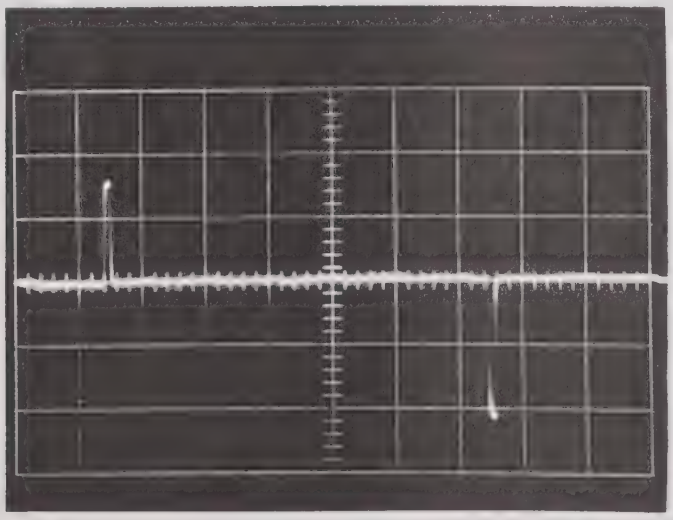


Figure VII-2. TWO SINGLE CHANNEL DISCONTINUITIES

Similarly, if the oscilloscope display is normal up to some point and then bad from that point to the end (Figure VII-3), the location of the transition point marks the defective Computer Board, and the problem is most likely a faulty shift register stage. It might be pointed out that by simply removing the bad Computer Board and then rearranging the remaining boards so that the "empty" socket is at the right hand end of the Computer Compartment, the instrument can continue to operate at 90% of its full capacity while the defective board is being repaired.

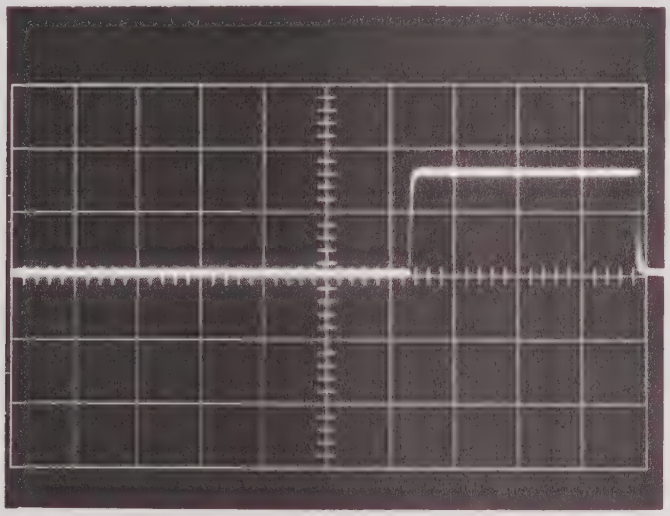


Figure VII-3. EFFECT OF FAULTY SHIFT REGISTER STAGE

By further checking it should be possible to determine which stage of the problem Computer Board is defective. To identify the stage responsible for a given discontinuity, take a ten megohm or higher resistor, and after grounding one end, touch the other end to that mounting post which is the junction of the time constant resistor and integrating capacitor of any stage. The corresponding pedestal should immediately show a negative shift.

If only one pedestal is affected, remove the time constant resistor of the defective stage and erase. If, after erasing, the pedestal seems to be more or less stationary near zero, one can conclude that the Readout Gate Transistor is probably good. Replace the time constant resistor, and, after erasing again, switch to Readout Only operation. If the pedestal goes positive, the Computation Gate Transistor, that between the common source of the two multiplier transistors and the time constant resistor may be leaky or shorted. If no such drift occurs, switch back to COR. $0<\tau<T$ operation, and after the observed pattern stabilizes, switch the B coupling Switch to GRD. If the pedestal moves negatively, the "+B" multiplier transistor for that stage is suspect. If the pedestal moves positively, the other multiplier transistor is probably defective. Needless to say, these are only a few of the possibilities which might be checked. Before doing any actual repair, bear in mind the earlier comments with reference to contacting PAR for advice.

7.9 OTHER CIRCUITS

If the problem is not in the Computer Section, use the following table(s) to isolate the problem to a particular board and circuit. Table VII-1 applies to both the Model 100 and the Model 101, while Table VII-2 applies to the Model 101 alone, if the instrument is a Model 101, make the checks indicated in Table VII-2 after completing those outlined in Table VII-1. Each signal specified is at the output of a given circuit. By proceeding in the indicated sequence, the missing or improper signal will identify the problem area. Bear in mind that although a missing or distorted signal in all likelihood means that the circuit producing the signal is at fault, it might happen that a defect in the following stage is loading the circuit, giving a possibly misleading indication.

EXCEPT THAT THE CHANNEL A COUPLING SWITCH SHOULD BE SET TO "CAL. 1V", THE FRONT PANEL CONTROLS SHOULD BE SET AS SPECIFIED UNDER "ISOLATING THE MALFUNCTION", PAGE VII-5.

CIRCUIT UNDER TEST	BOARD	WHERE	PULSE OFF	PULSE ON	DURATION	PERIOD
T-Clock	T-Clock	Pin 8	+1 V	-6 V	0.1 µs	1 µs
Ch. A Preamp.	Quantizer	A Test Pt.	+2.0 V	(no pulse)		
Quantizer	Quantizer	Pin 22	-4.4 V	-5 V	0.2 µs	0.3 µs
Quantizer	Quantizer	Pin 21	-4.4 V	-5 V	0.1 µs	0.3 µs
Sampler	Sampler	Pins 1 & 2	+1 V	-3 V	0.1 µs	random multiples of one microsecond
Ch. B Preamp.	Ch. B Amp.	B Test Pt.	+1.5 V	(no pulse)		
Channel B	Ch. B Amp.	Pin 22	+9.2 V	(no pulse)		
Channel B	Ch. B Amp.	Pin 21	+6.2 V	(no pulse)		
Readout Only	Output Buffer	Pin 13	+0.7 V	(no pulse)		
Readout Clk.	Programmer	Pin 8	-11 V	-1 V	10 µs	0.5 ms
Count. Trig.	Output Buffer	Pin 14	-12 V	-2 V	10 µs	0.5 ms
Units Counter	Counter	Pins 13-22, 34 & 35	+11 V	0 V	0.5 ms	5.0 ms
Tens Counter	Counter	Pins 2-11	+11 V	0 V	5.0 ms	60 ms
Start/Finish	Output Buffer	Pin 4	+1 V	+11 V	50 ms	60 ms
Zero Command	Programmer	Pin 12	+12 V	0 V	5.5 ms	60 ms
τ=0 Command	Programmer	Pin 18	+11 V	0 V	5.0 ms	60 ms
Output Amp.	Output Buffer	Pin 34	0 V	+2 V	55 ms	60 ms
Output Amp.	Output Buffer	Pin 24	0 V	+1 V	55 ms	60 ms

Table VII-1. TROUBLESHOOTING VOLTAGES AND WAVEFORMS

FOLLOWING CHECKS APPLY TO MODEL 101 ONLY, DIGITAL DELAY LINE BOARD (DI 2685) MOUNTED BELOW COMPUTER SECTION UNDER CHASSIS

CIRCUIT UNDER TEST	BOARD	WHERE	PULSE OFF	PULSE ON	DURATION	PERIOD
Clock Shaper	Dig. Dly. Line	Test Point	-1 V	-12 V	0.3 to 0.7 μs	1 μs
Input Driver	" " "	Either end of K1102	0 V	-12 V	random multiples of	1 μs
Output Schmitt	" " "	Terminal marked "COMP A 27"	+0.7 V	-3 V	random multiples of	1 μs
SET COMPUTATION PERIOD SWITCH TO ".2 m SEC." and PRECOMPUTATION PERIOD SWITCH TO "T".						
K1101	Dig. Dly. Line	Test Point	-1 V	-12 V	.8 μs to 1.3 μs	2 μs
SR1101 through SR1105	" " "	COMP A 27	+0.7 V	-3 V	random multiples of	2 μs
WHILE CONTINUING TO MONITOR "COMP A 27", ADVANCE THE PRECOMPUTATION PERIOD SWITCH ONE STEP TO SWITCH IN THE NEXT FIVE SHIFT REGISTER MODULES (SR1106 thru SR1110). IF NO CHANGE IN THE OBSERVED WAVEFORM IS NOTED, THESE MODULES ARE FUNCTIONING PROPERLY. IN LIKE MANNER CONTINUE TO ADVANCE THE PRECOMPUTATION PERIOD SWITCH ONE STEP AT A TIME TO CHECK EACH CONSECUTIVE SET OF FIVE MODULES. AFTER ALL MODULES HAVE BEEN CHECKED, RESET THE COMPUTATION PERIOD AND PRECOMPUTATION SWITCHES TO ".1 mSEC." and "0" RESPECTIVELY.						
Output Schmitt	Dig. Dly. Line	COMP A 28	+0.7 V	-3 V	random multiples of	1 μs

Table VII-2. TROUBLESHOOTING VOLTAGES AND WAVEFORMS WHICH APPLY TO MODEL 101 ONLY

SECTION VIII
WARRANTY

Princeton Applied Research Corporation warrants each instrument of its own manufacture to be free from defects in material and workmanship. Obligations under this Warranty are limited to replacing, repairing or giving credit for the purchase price, at our option, of any instrument returned prepaid to our factory for that purpose within ONE year of delivery to original purchaser. Instruments returned to the factory are accepted only when prior authorization has been given by an authorized representative of Princeton Applied Research Corporation.

This Warranty shall not apply to any instrument, which our inspection shall disclose to our satisfaction, to have become defective or unworkable due to abuse, mishandling, misuse, accident, alteration, negligence, improper installation, or other causes beyond our control.

Princeton Applied Research Corporation reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

This Warranty is in lieu of, and excludes all other warranties or representations, expressed, implied or statutory, and all other obligations or liabilities of Princeton Applied Research Corporation including special or consequential damages, and no other source is authorized to assume for Princeton Applied Research Corporation any other liability.

SECTION IX
SCHEMATICS

Page

IX-1 ---------- TABLE OF SCHEMATICS AND LAYOUT DIAGRAMS

IX-2 ---------- BLOCK DIAGRAM

IX-3 ---------- SIGNAL FLOW DIAGRAM

IX-4 ---------- QUANTIZER BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-5 ---------- SAMPLER BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-6 ---------- T-CLOCK BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-7 ---------- CHANNEL B AMPLIFIER BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-8 ---------- DIGITAL DELAY LINE BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-9 ---------- COMPUTER BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-10 ---------- PROGRAMMER BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-11 ---------- COUNTER BOARD SCHEMATIC AND LAYOUT DIAGRAM

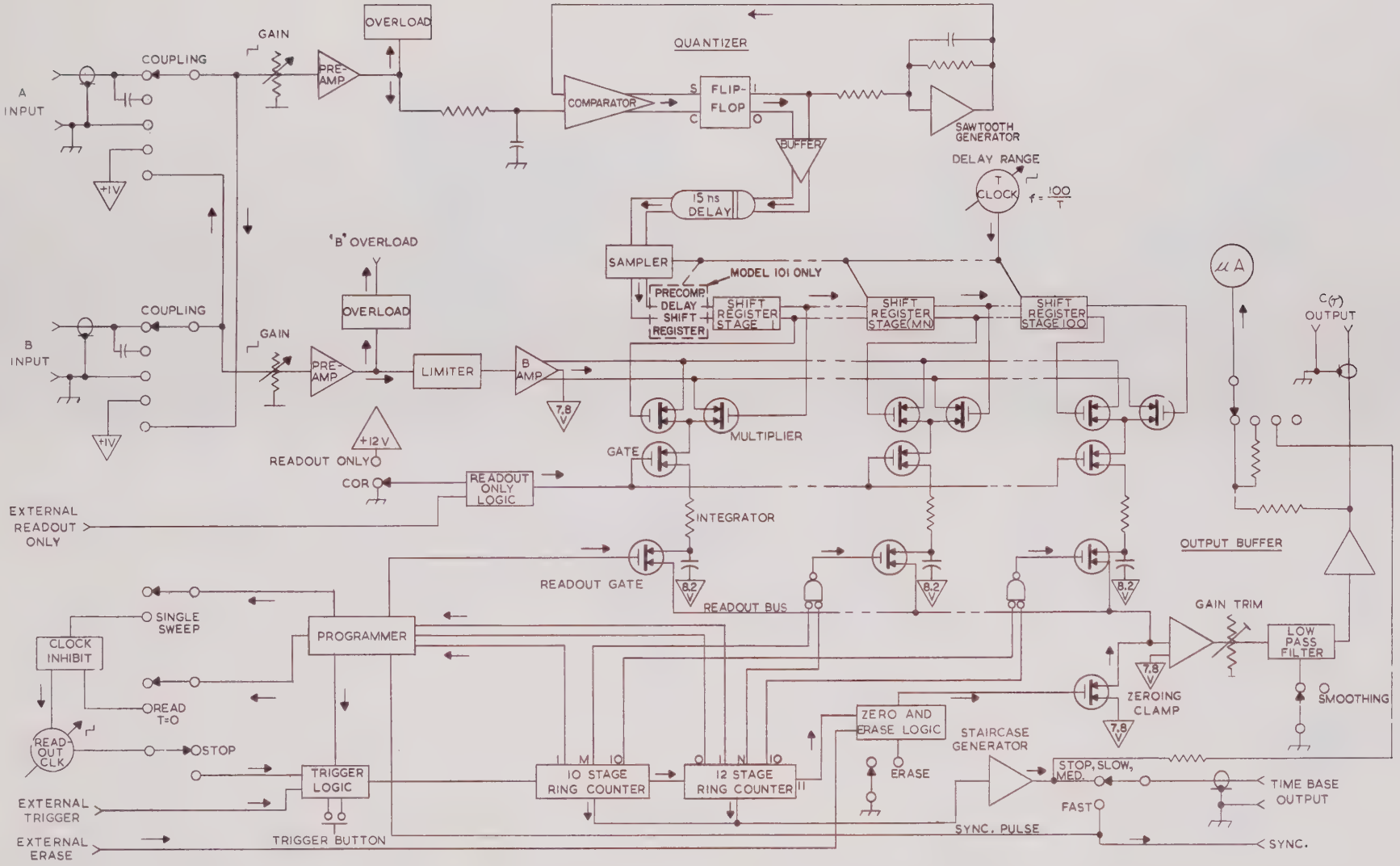
IX-12 ---------- OUTPUT BUFFER BOARD SCHEMATIC AND LAYOUT DIAGRAM

IX-13 ---------- POWER SUPPLY I & II SCHEMATIC AND LAYOUT DIAGRAM

IX-14 ---------- POWER SUPPLY III SCHEMATIC AND LAYOUT DIAGRAM

IX-15 ---------- CHASSIS WIRING DIAGRAM (Model 100)

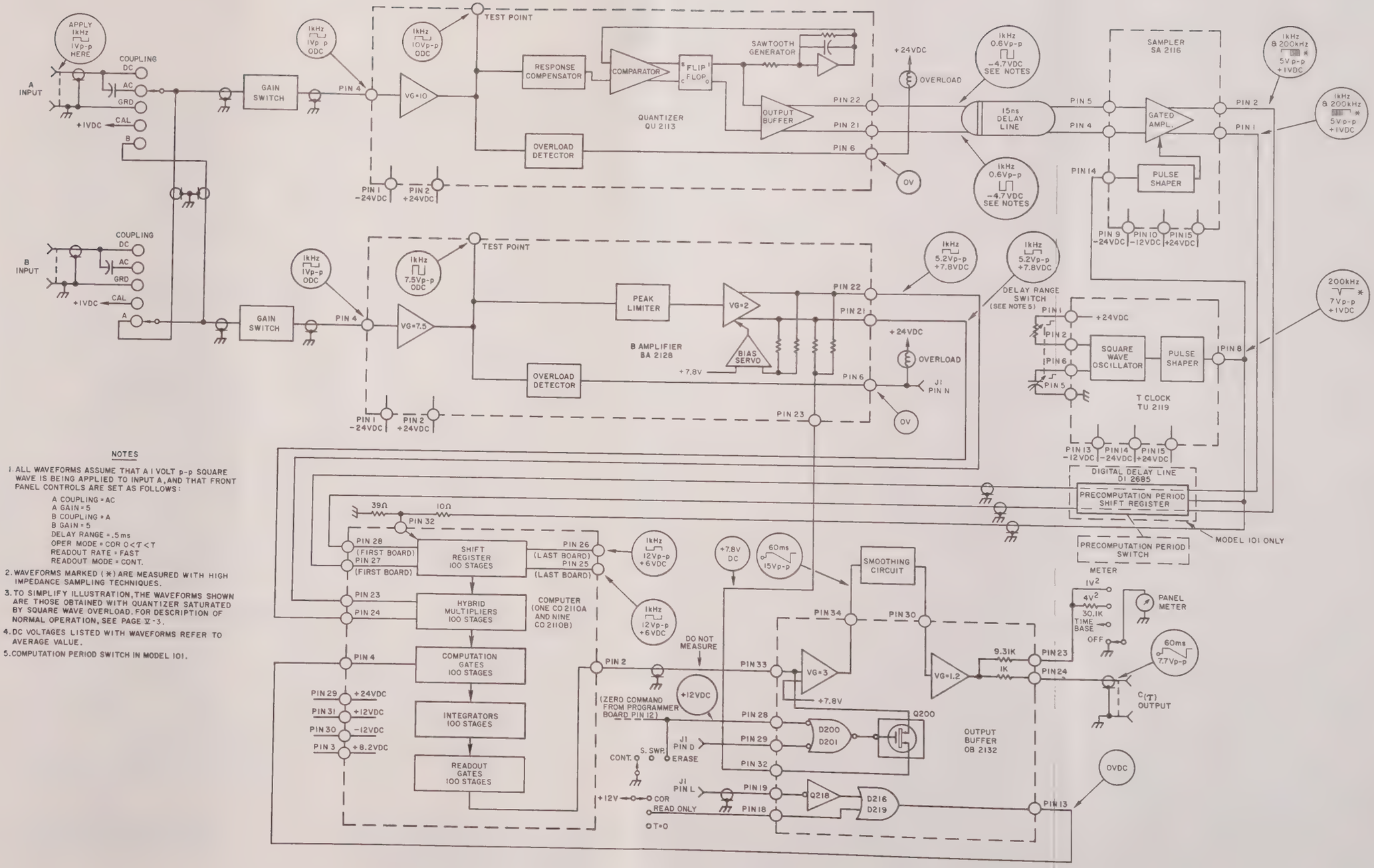
IX-16 ---------- CHASSIS WIRING DIAGRAM (Model 101)



BLOCK DIAGRAM MODEL 100 AND MODEL 101

COPYRIGHT 1967 BY PRINCETON APPLIED RESEARCH CORPORATION. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.

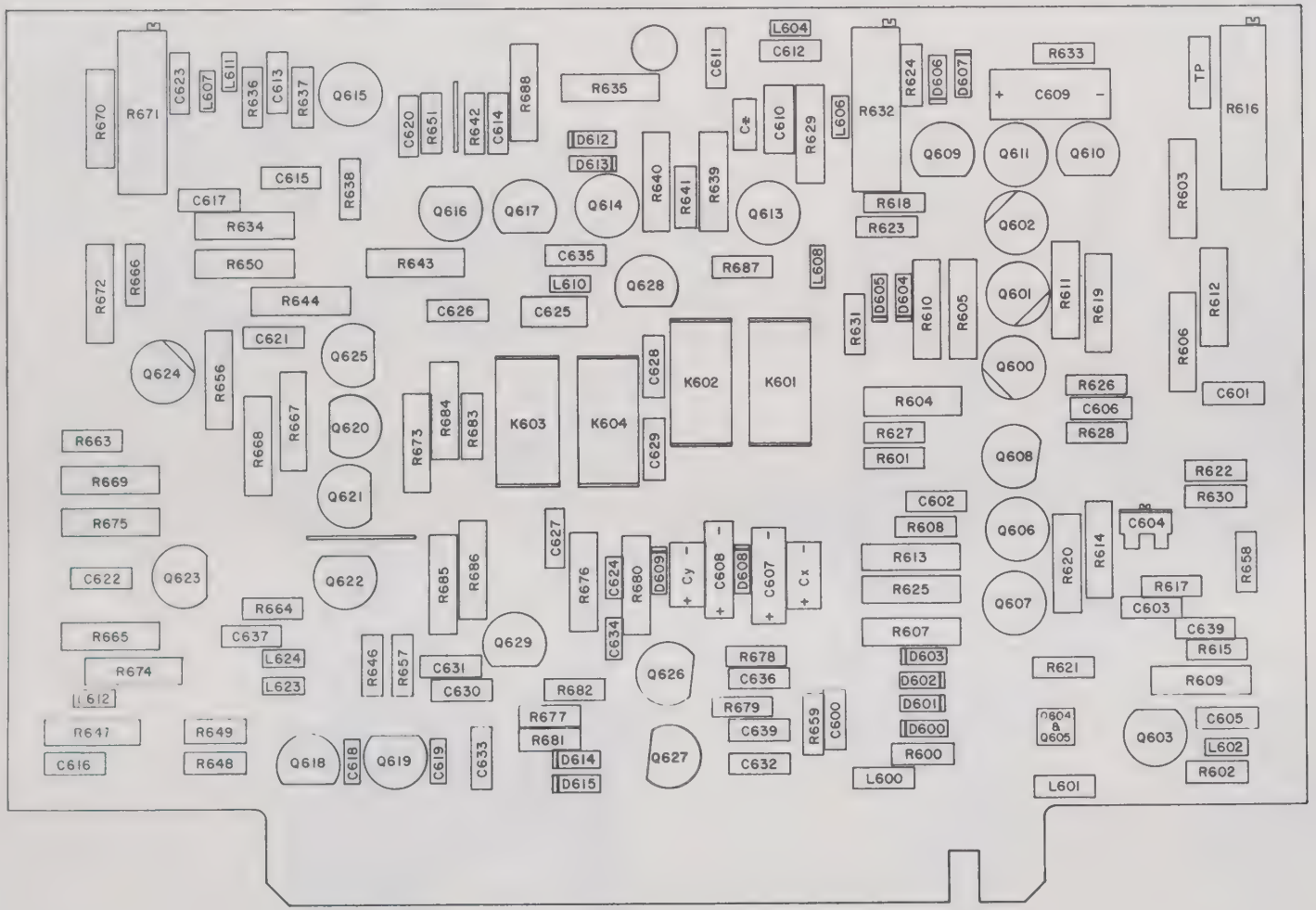
2145 C SD A



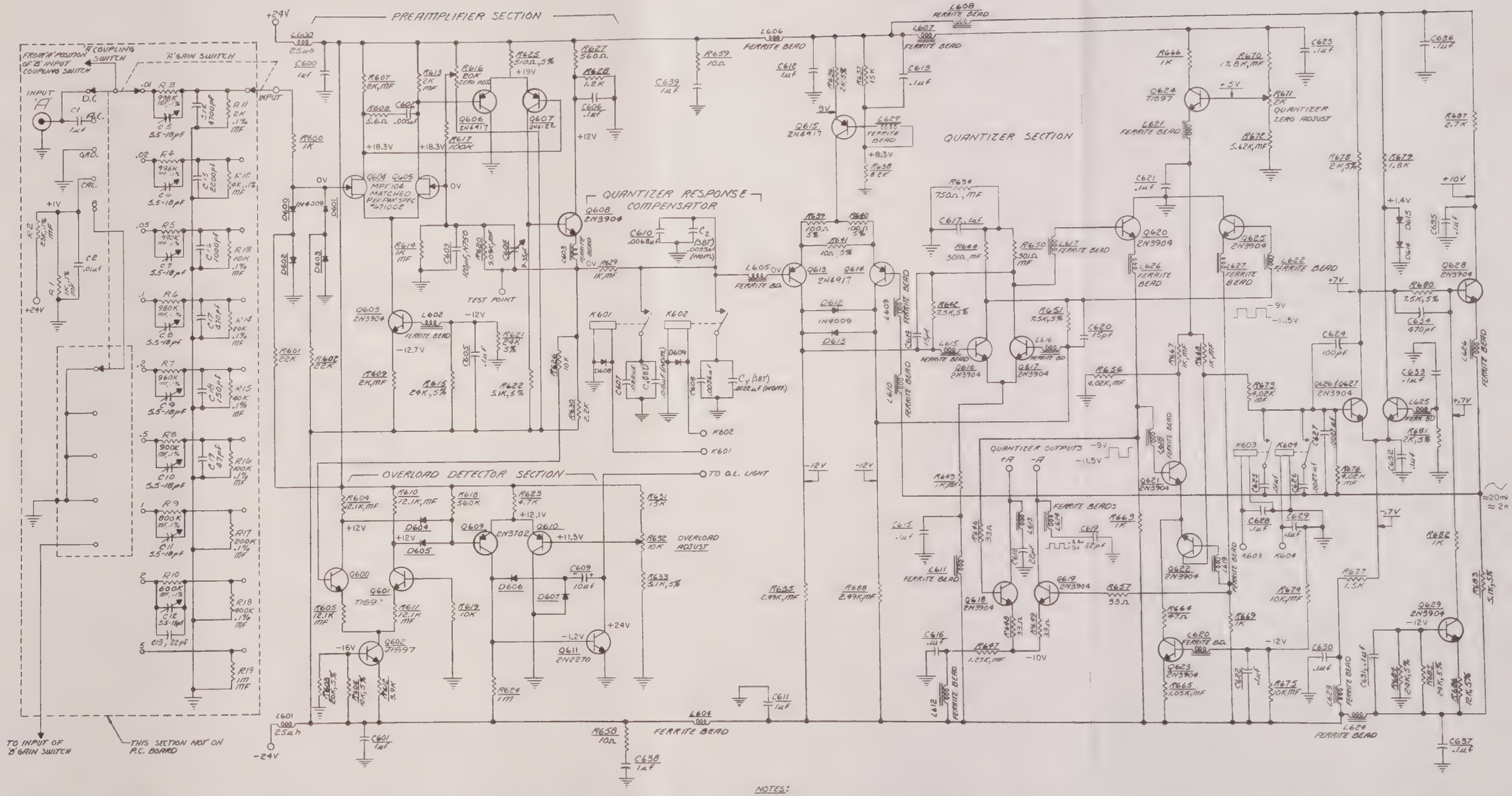
NOTES

1. ALL WAVEFORMS ASSUME THAT A 1 VOLT p-p SQUARE WAVE IS BEING APPLIED TO INPUT A, AND THAT FRONT PANEL CONTROLS ARE SET AS FOLLOWS:
   - A COUPLING = AC
   - A GAIN = 5
   - B COUPLING = A
   - B GAIN = 5
   - DELAY RANGE = .5 ms
   - OPER MODE = COR $0 < T < T$
   - READOUT RATE = FAST
   - READOUT MODE = CONT.
2. WAVEFORMS MARKED (*) ARE MEASURED WITH HIGH IMPEDANCE SAMPLING TECHNIQUES.
3. TO SIMPLIFY ILLUSTRATION, THE WAVEFORMS SHOWN ARE THOSE OBTAINED WITH QUANTIZER SATURATED BY SQUARE WAVE OVERLOAD. FOR DESCRIPTION OF NORMAL OPERATION, SEE PAGE IX-3.
4. DC VOLTAGES LISTED WITH WAVEFORMS REFER TO AVERAGE VALUE.
5. COMPUTATION PERIOD SWITCH IN MODEL 101.

SIGNAL FLOW DIAGRAM
MODEL 100 & 101



QUANTIZER BOARD LAYOUT DIAGRAM



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
+24	+24	GRD.	IN	N.C.	O.L.	FAST READOUT	SLOW READOUT	GRD.	GRD.	GRD.	GRD.	GRD.	GRD.	GRD.	GRD.	GRD.	GRD.	GRD.	GRD.	A-	A+	GRD.

PIN CONNECTIONS

NOTES:

1- ALL RESISTORS ½ WATT 10% UNLESS OTHERWISE NOTED.

2- ALL DIODES IN4828 UNLESS OTHERWISE NOTED.

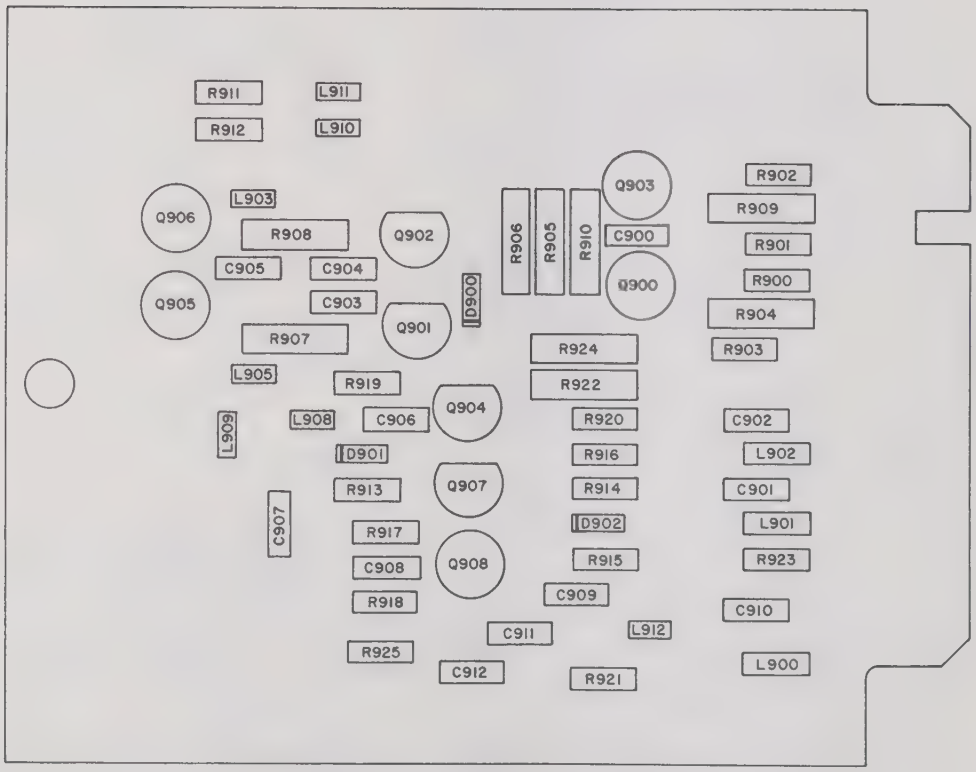
3- ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:

(a) A&B GAIN _ _ _ _ _ _ 1
(b) A&B COUPLING _ _ _ GRD.
(c) DELAY RANGE _ _ _ 10mSEC.
(d) OPERATION MODE _ _ _ COR 0<T<T
(e) READOUT RATE _ _ _ FAST
(f) READOUT MODE _ _ _ CONT.

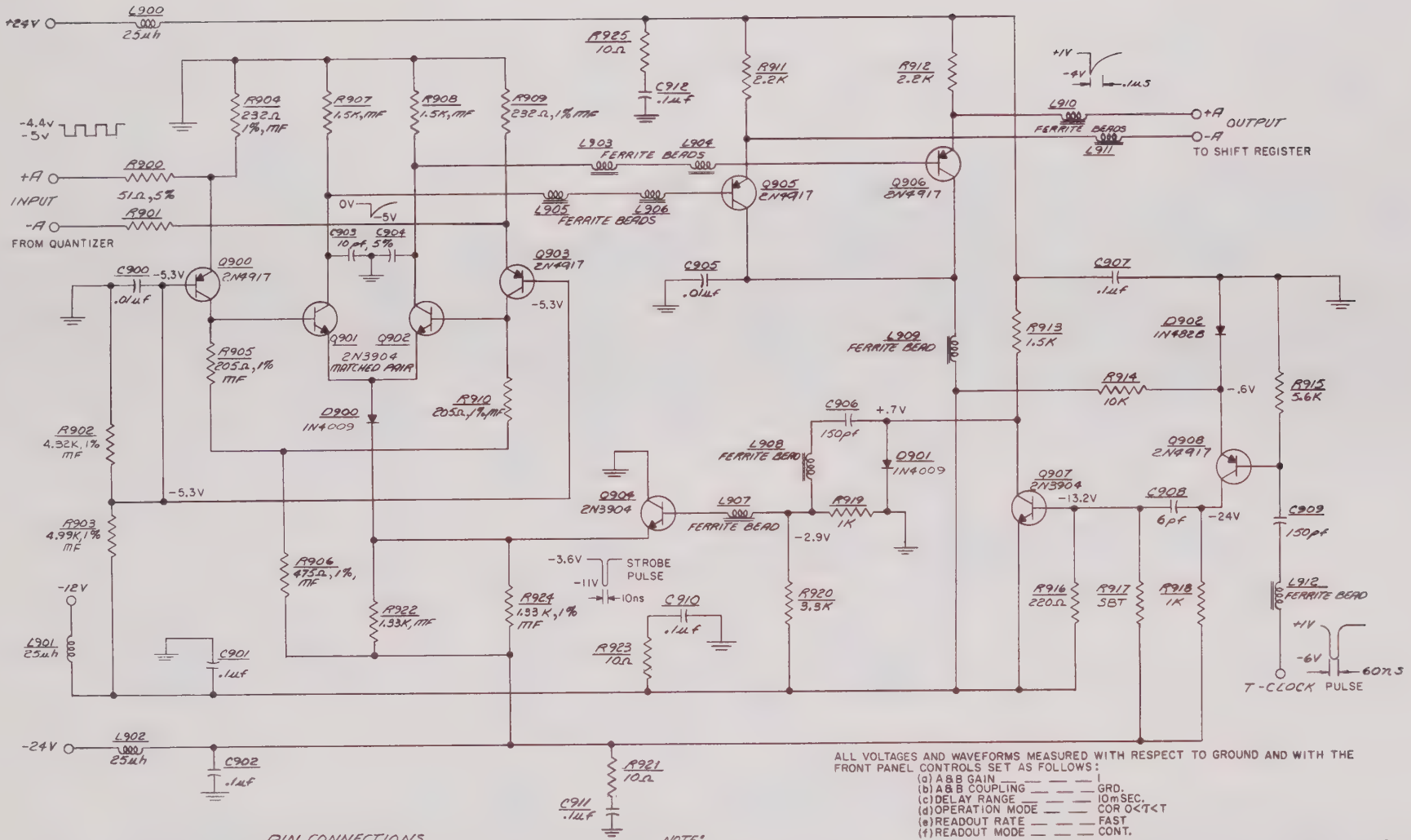
COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORPORATION. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.

QUANTIZER BD. SCHEMATIC

MODEL 100 AND 101 CIRCUIT BD.** QU 2113



SAMPLER BOARD LAYOUT DIAGRAM



ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:

(a) A&B GAIN — — — 1
(b) A&B COUPLING — — — GRD.
(c) DELAY RANGE — — — 10mSEC.
(d) OPERATION MODE — — COR O<T<T
(e) READOUT RATE — — — FAST
(f) READOUT MODE — — — CONT.

PIN CONNECTIONS

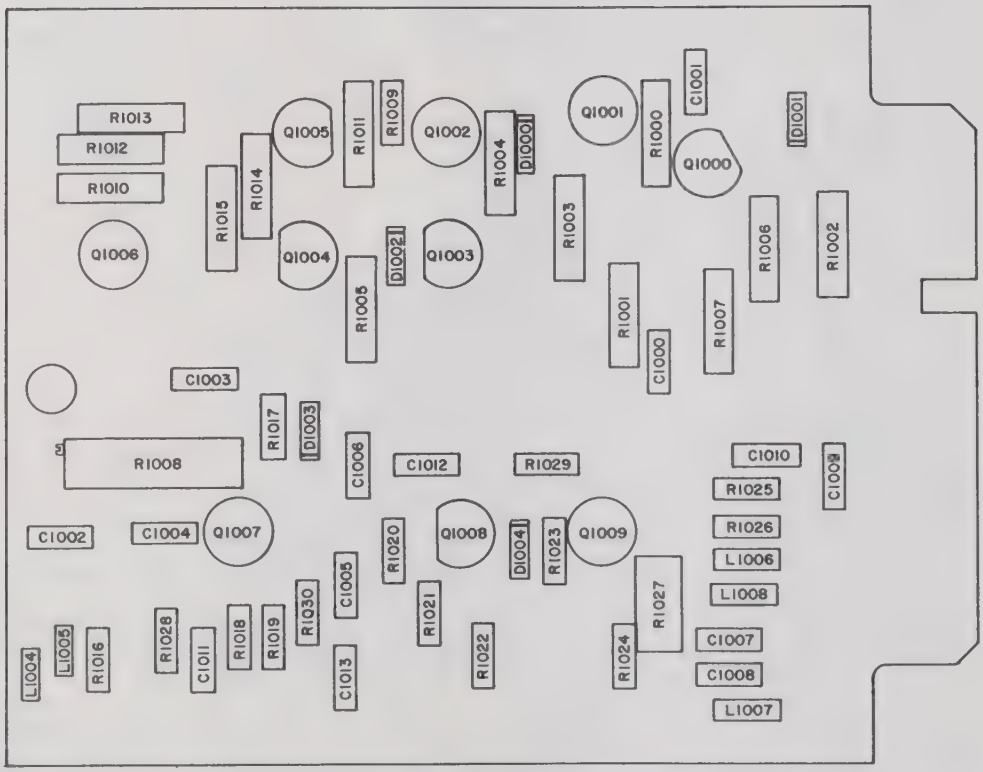
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
-A OUT	+A OUT	GRD.	-A IN	+A IN	GRD.	GRD.	GRD.	-24	-12	GRD.	GRD.	GRD.	T-CLK.	+24

NOTE:
1- ALL RESISTORS ½ W, 5% COMP. UNLESS OTHERWISE NOTED.

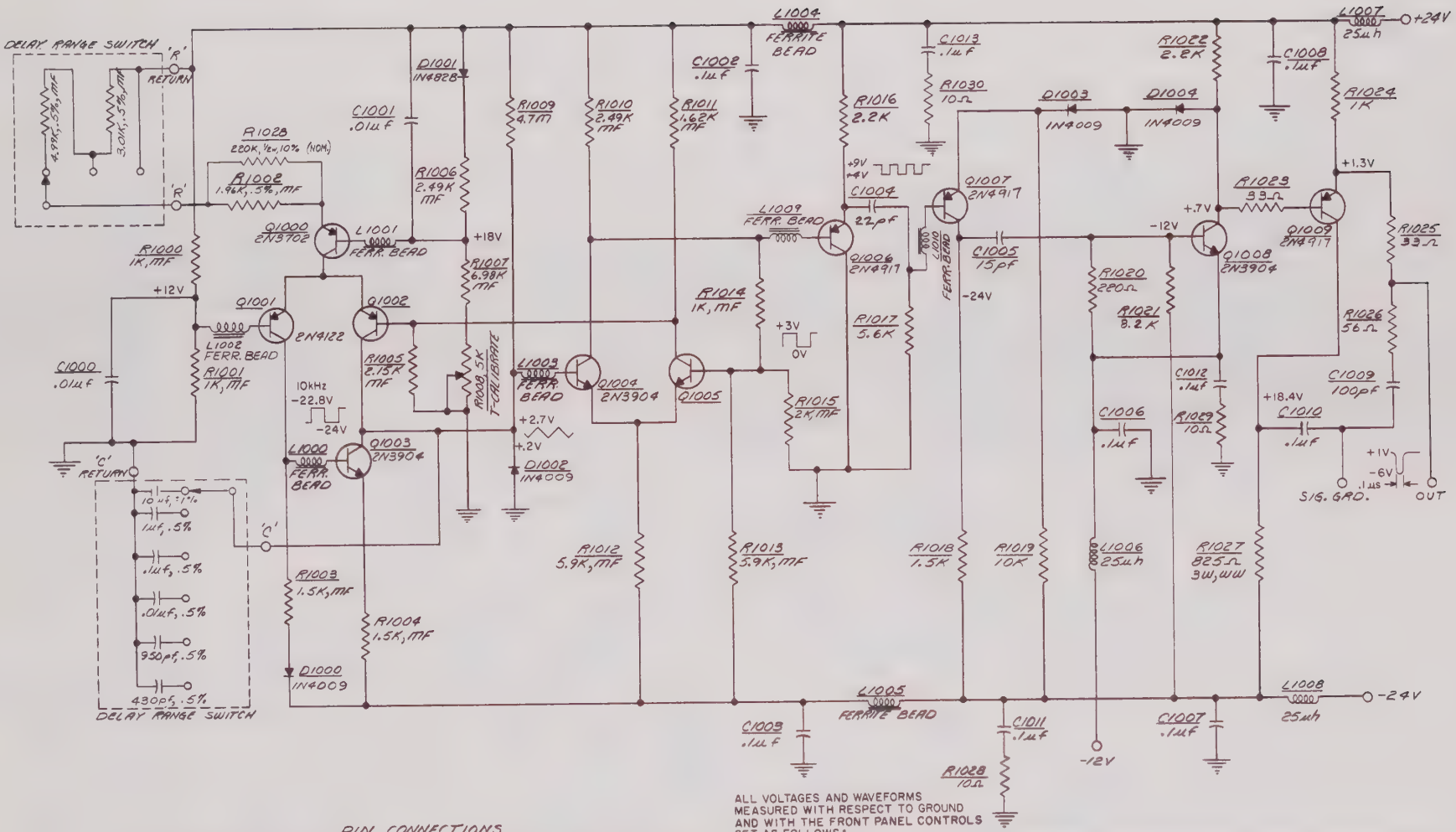
COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.

SAMPLER BD. SCHEMATIC — MODEL 100 AND 101 — CIRCUIT BD.** SA 2116

2301 | C | SD | E1



T CLOCK BOARD LAYOUT DIAGRAM



PIN CONNECTIONS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RES. MTH.	RES. SW.	GRD.	GRD.	GRD.	COM. SW.	GRD.	OUT	SIG. GRD.	SIG. GRD.	GRD.	GRD.	-12	-24	+24

ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:

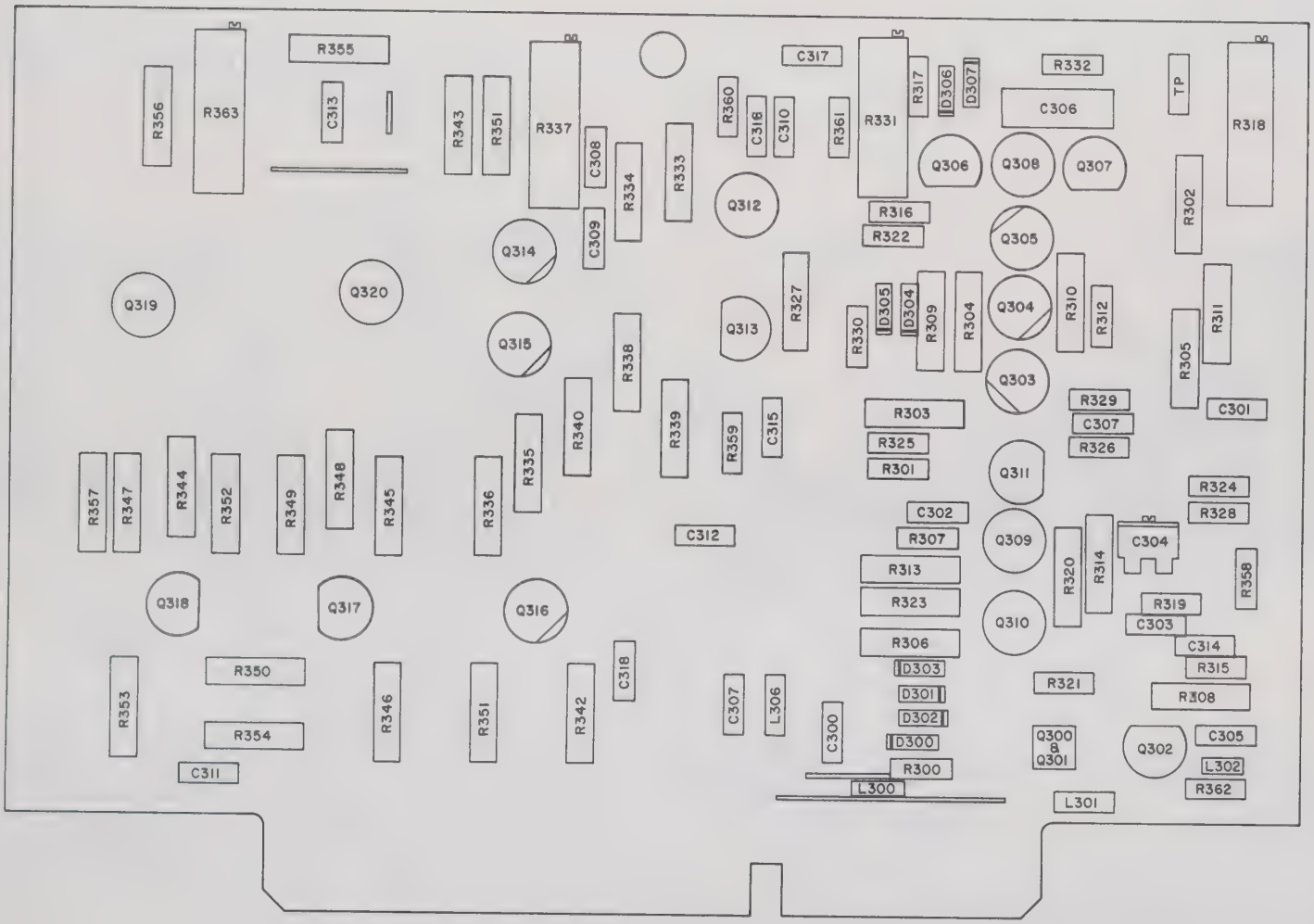
(a) A&B GAIN — — — 1
(b) A&B COUPLING — — GRD.
(c) DELAY RANGE — — 10mSEC.
(d) OPERATION MODE — COR 0<T<T
(e) READOUT RATE — — FAST
(f) READOUT MODE — — CONT.

T-CLOCK BD. SCHEMATIC MODEL-100 AND 101

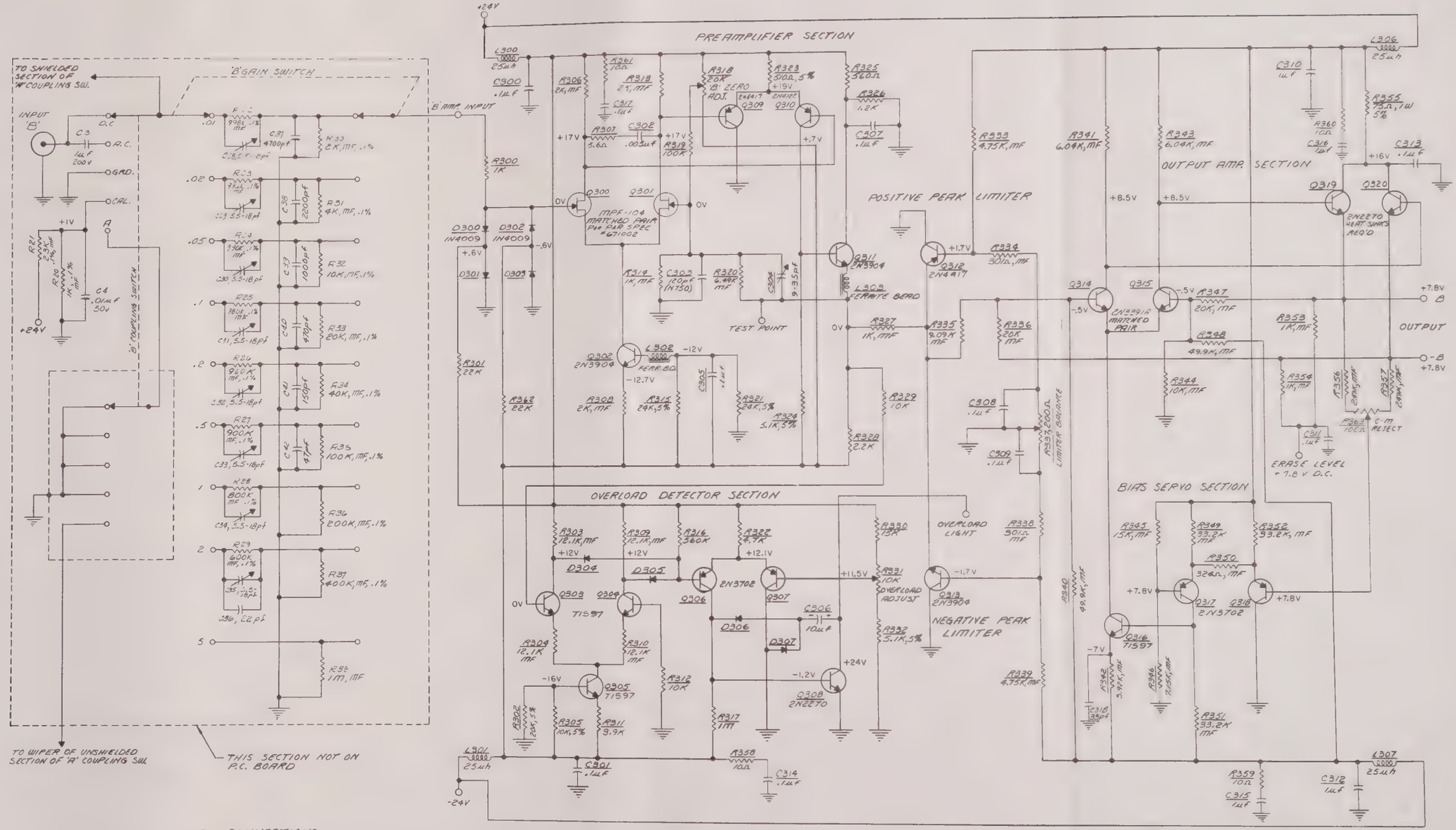
CIRCUIT BD.# TU2119

COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.

2300 C SD F



B AMPLIFIER BOARD LAYOUT DIAGRAM



PIN CONNECTIONS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
-24	+24	GRD	B IN	GRD	0.1 VOLT	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	GRD	-B	+B	CASE (HI-Z)

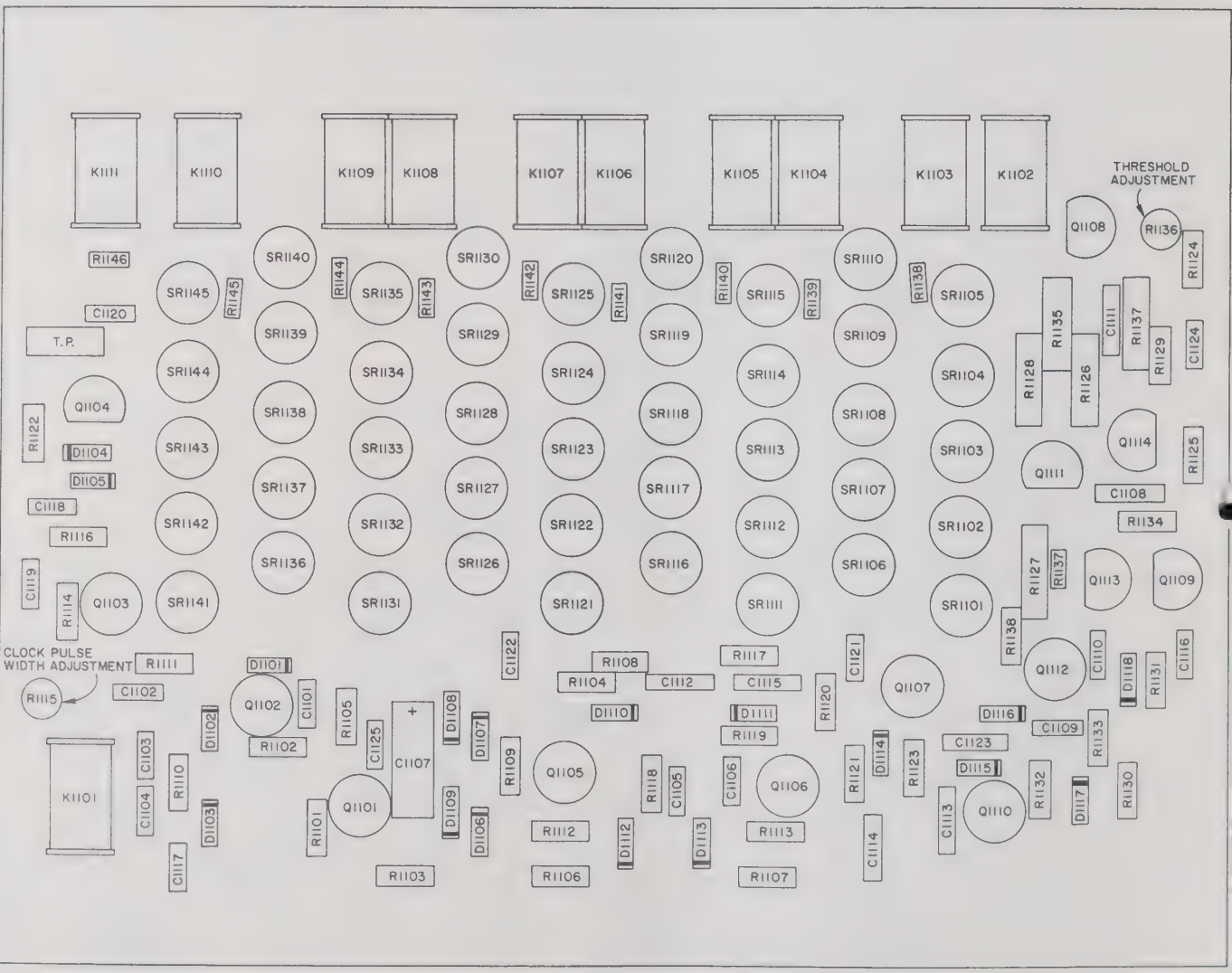
NOTES:
1- ALL RESISTORS 1/2 WATT 10% COMP. UNLESS OTHERWISE NOTED.
2- ALL DIODES IN4820 UNLESS OTHERWISE NOTED.

ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:
(a) A&B GAIN ____ _ _ _ _ _ _ _ |
(b) A&B COUPLING _ _ _ _ GRD.
(c) DELAY RANGE ____ _ _ _ 10mSEC.
(d) OPERATION MODE _ _ _ _ COR D◁T◁T
(e) READOUT RATE _ _ _ _ FAST
(f) READOUT MODE ____ _ _ _ CONT.

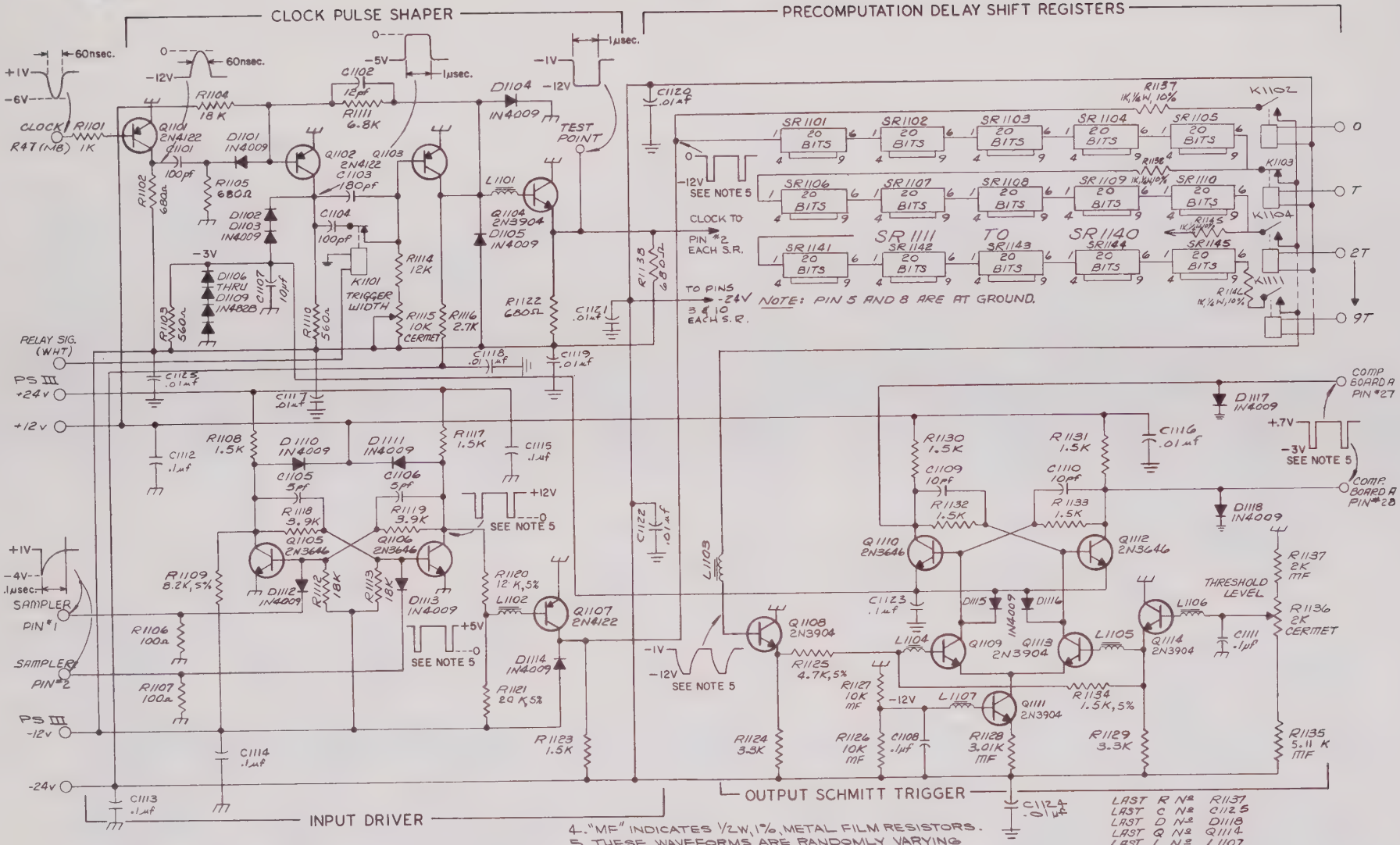
COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORP
THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.

CHANNEL 'B' AMPLIFIER BD. SCHEMATIC

MODEL 100 AND 101 CIRCUIT BD.# BA 2128



DIGITAL DELAY LINE LAYOUT DIAGRAM



NOTES:

1. ALL FERRITE BEADS INSTALLED ON BASE LEAD.
2. THE TOTAL DELAY CAPACITY OF THE CIRCUIT DEPENDS ON THE NUMBER OF SHIFT REGISTER MODULES USED. THE MAXIMUM IS 45 MODULES OR A TOTAL OF 900 BITS.
3. ALL RESISTORS ½ w, 10%, COMP. UNLESS OTHERWISE NOTED.
4. "MF" INDICATES ½W, 1%, METAL FILM RESISTORS.
5. THESE WAVEFORMS ARE RANDOMLY VARYING IN FREQUENCY AND SYMETRY.
6. ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:
   - (a) A & B GAIN ——— I
   - (b) A & B COUPLING ——— GRD.
   - (c) COMPUTATION PERIOD ——— 10mSEC.
   - (d) PRECOMPUTATION PERIOD ——— T
   - (e) OPERATION MODE ——— COR (T)
   - (f) READOUT RATE ——— FAST
   - (g) READOUT MODE ——— CONT.

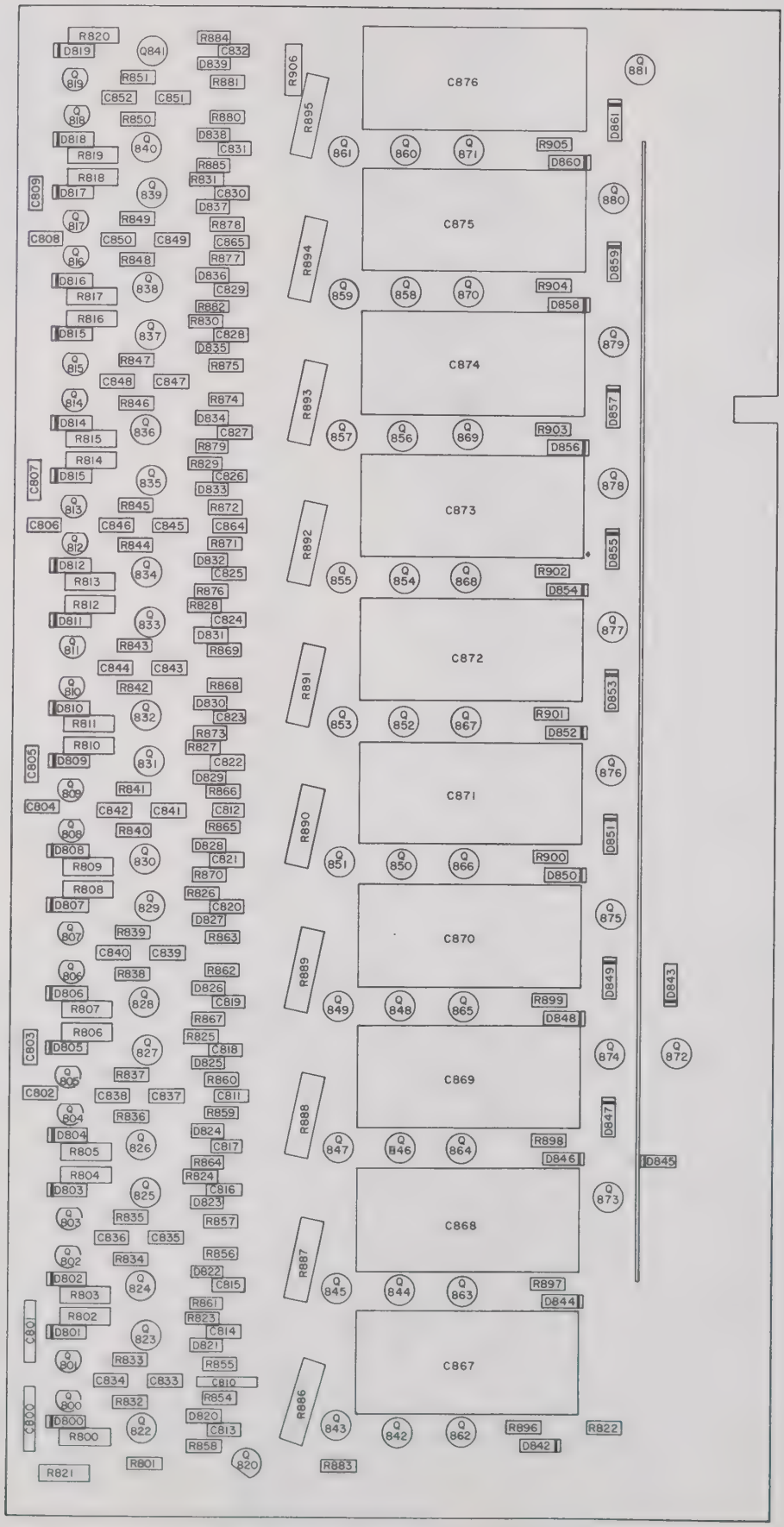
LAST R Nº R1137
LAST C Nº C1125
LAST D Nº D1118
LAST Q Nº Q1114
LAST L Nº L1107
LAST K Nº K1105

DIGITAL DELAY LINE SCHEMATIC

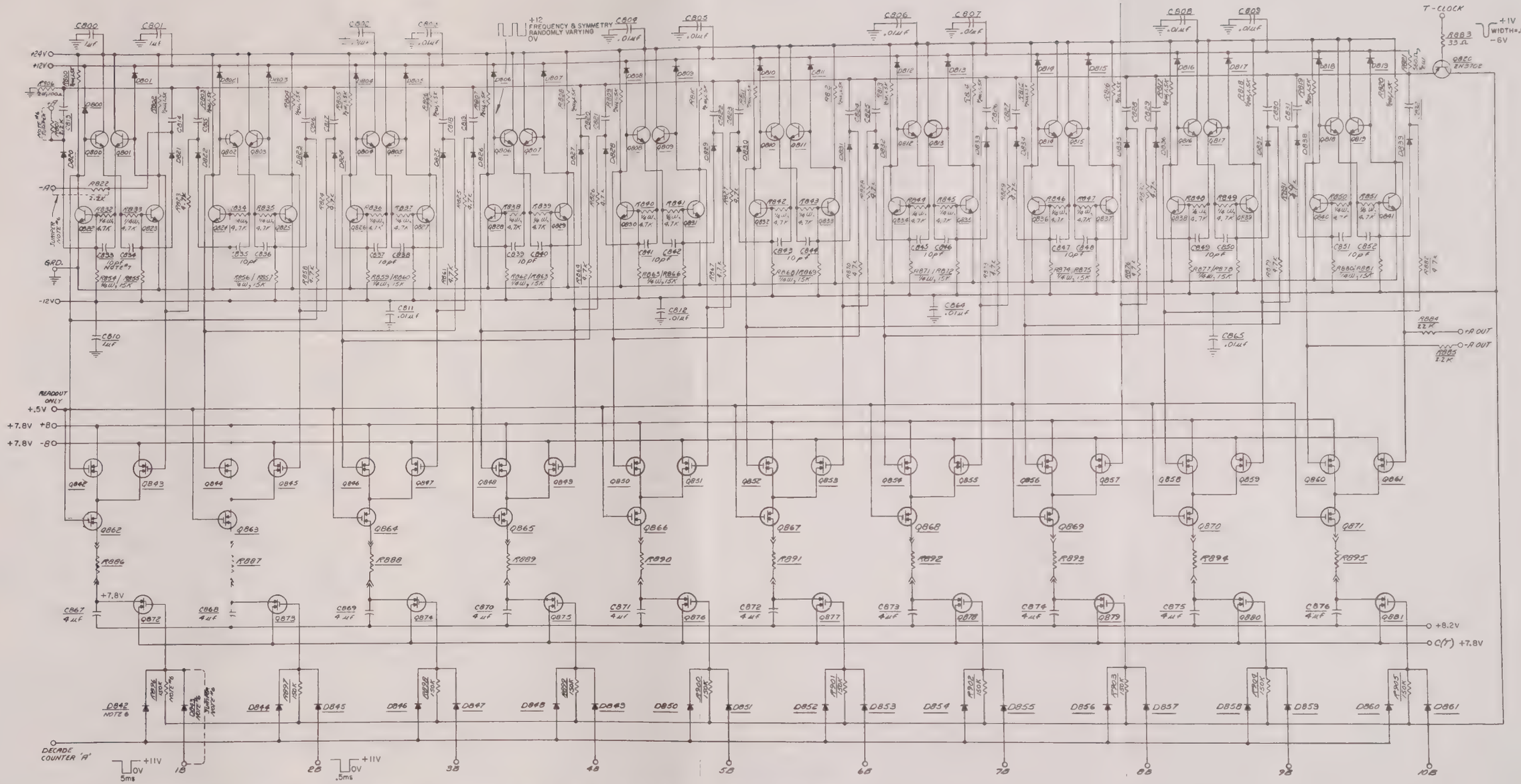
MODEL-101

BD. # D1 2685

COPYRIGHT 1967 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED, OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORP.



COMPUTER BOARD LAYOUT DIAGRAM



PIN CONNECTIONS

NOTES:

1. ALL RESISTORS 1/4 WATT 10% COMPOSITION UNLESS OTHERWISE NOTED.
2. Q800 TO Q839 TO BE IN4009; Q842 TO Q861 TO BE IN4822B.
3. Q800 TO Q819 TO BE 2N3904; Q822 TO Q841 TO BE 2N3646.
4. Q842 TO Q861 TO MEET REQUIREMENTS OF PAR SPEC.# 660902.
5. Q862 TO Q881 TO MEET REQUIREMENTS OF PAR SPEC.# 660111(B).
6. OMIT C813, C814, R801, R822, R896, D842 & D843 FROM COMPUTER BOARD 'A', & INSTALL JUMPERS WHERE INDICATED.
7. C833 & C834 TO BE 5pf ON COMPUTER BOARD 'A'.
8. C813 TO C832 TO BE 68pf.
9. R823 & R858 TO BE 1.5K ON COMPUTER 'A' BD. ONLY.

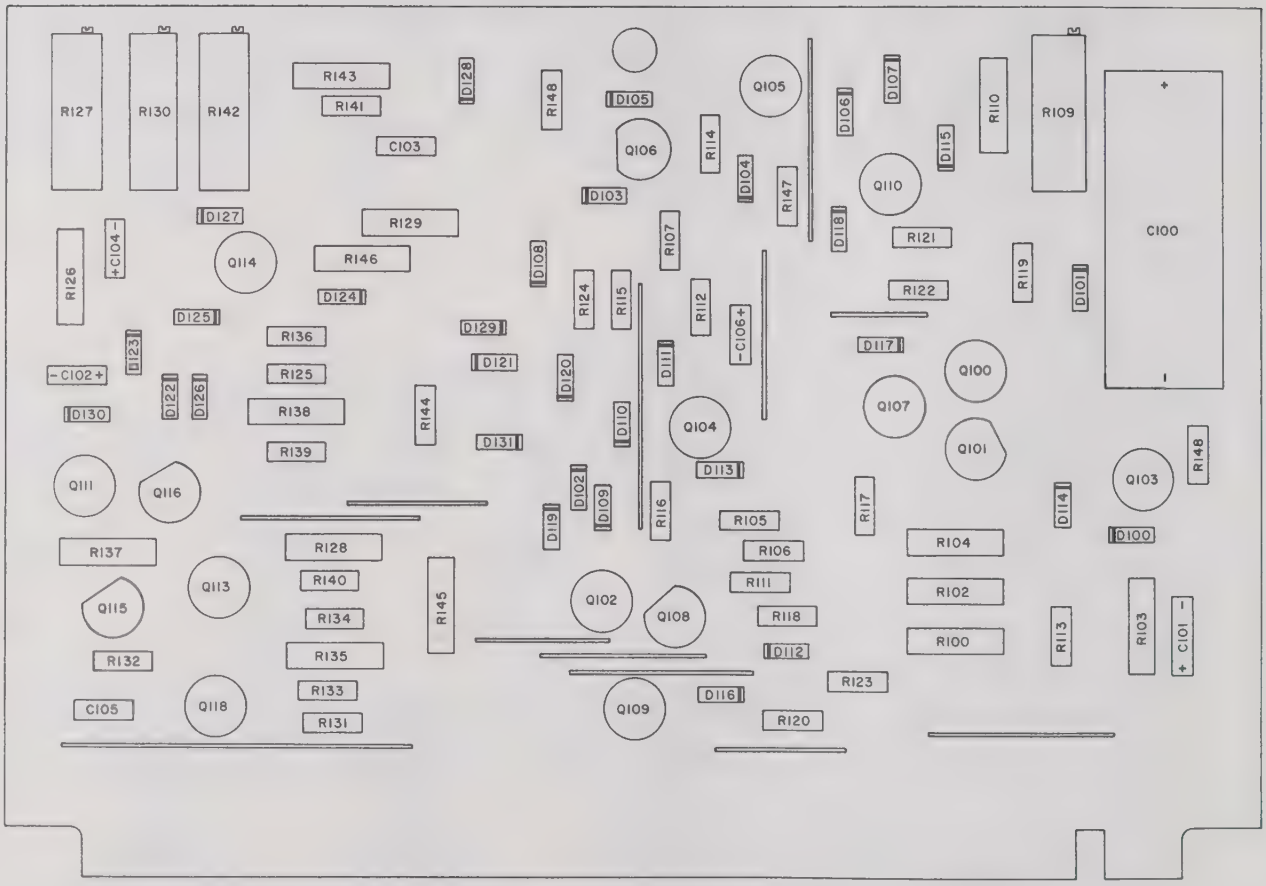
COMPUTER BD. SCHEMATIC — MODEL 100 AND 101

CIRCUIT BD. # CO 2110AB

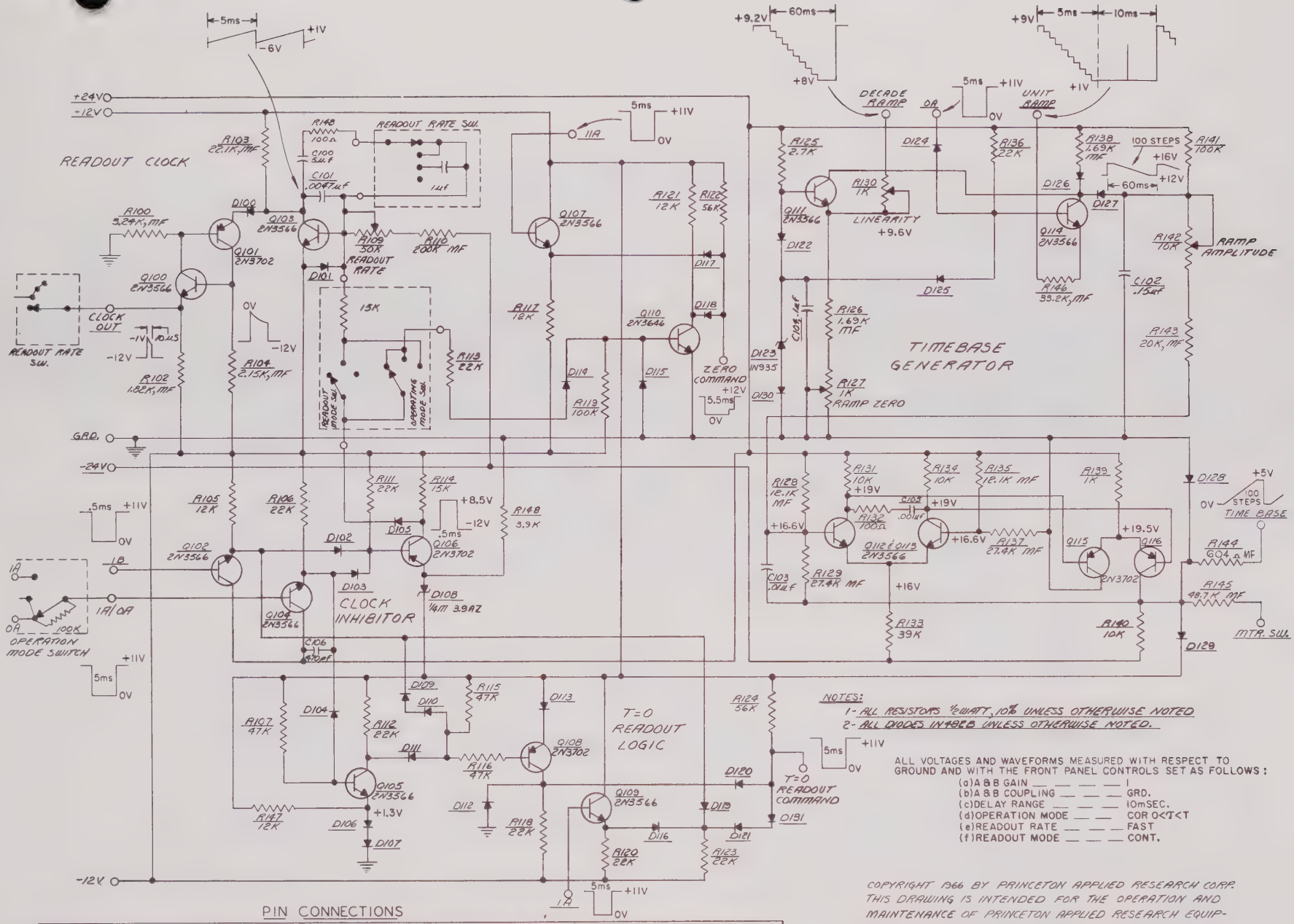
ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:

(a) A&B GAIN ___ ___ ___ ___ ___ 1
(b) A&B COUPLING ___ ___ ___ GRD.
(c) DELAY RANGE ___ ___ ___ 10mSEC.
(d) OPERATION MODE ___ ___ ___ COR 0<T<T
(e) READOUT RATE ___ ___ ___ FAST
(f) READOUT MODE ___ ___ ___ CONT.

COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORPORATION. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.



PROGRAMMER BOARD LAYOUT DIAGRAM

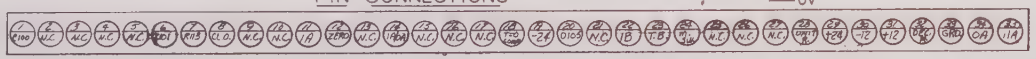


NOTES:
1- ALL RESISTORS ½ WATT, 10% UNLESS OTHERWISE NOTED
2- ALL DIODES IN4826 UNLESS OTHERWISE NOTED.

ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:

(a) A & B GAIN — — — — I
(b) A & B COUPLING — — — — GRD.
(c) DELAY RANGE — — — — 10mSEC.
(d) OPERATION MODE — — — — COR 0<T<T
(e) READOUT RATE — — — — FAST
(f) READOUT MODE — — — — CONT.

PIN CONNECTIONS

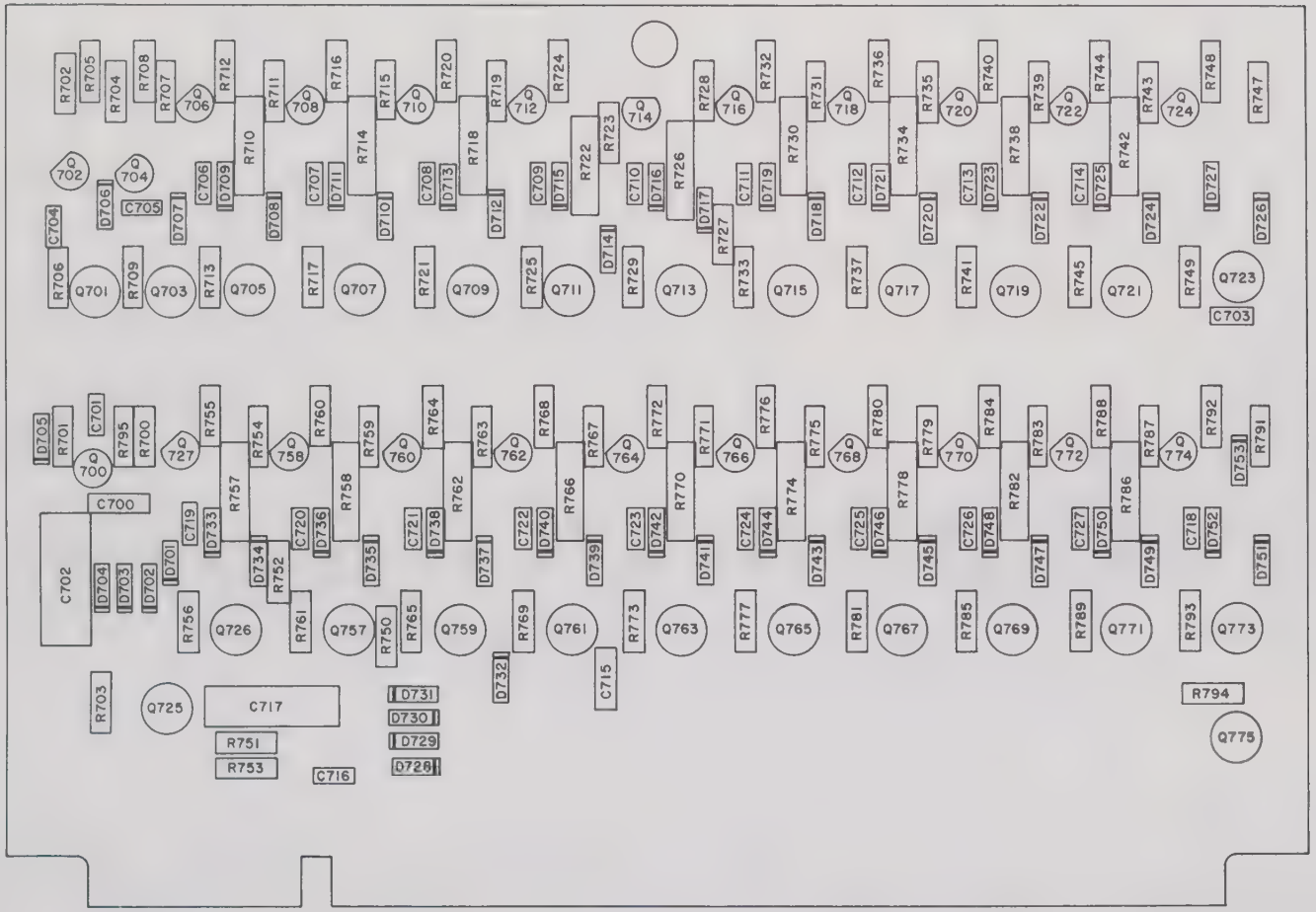


IX-10

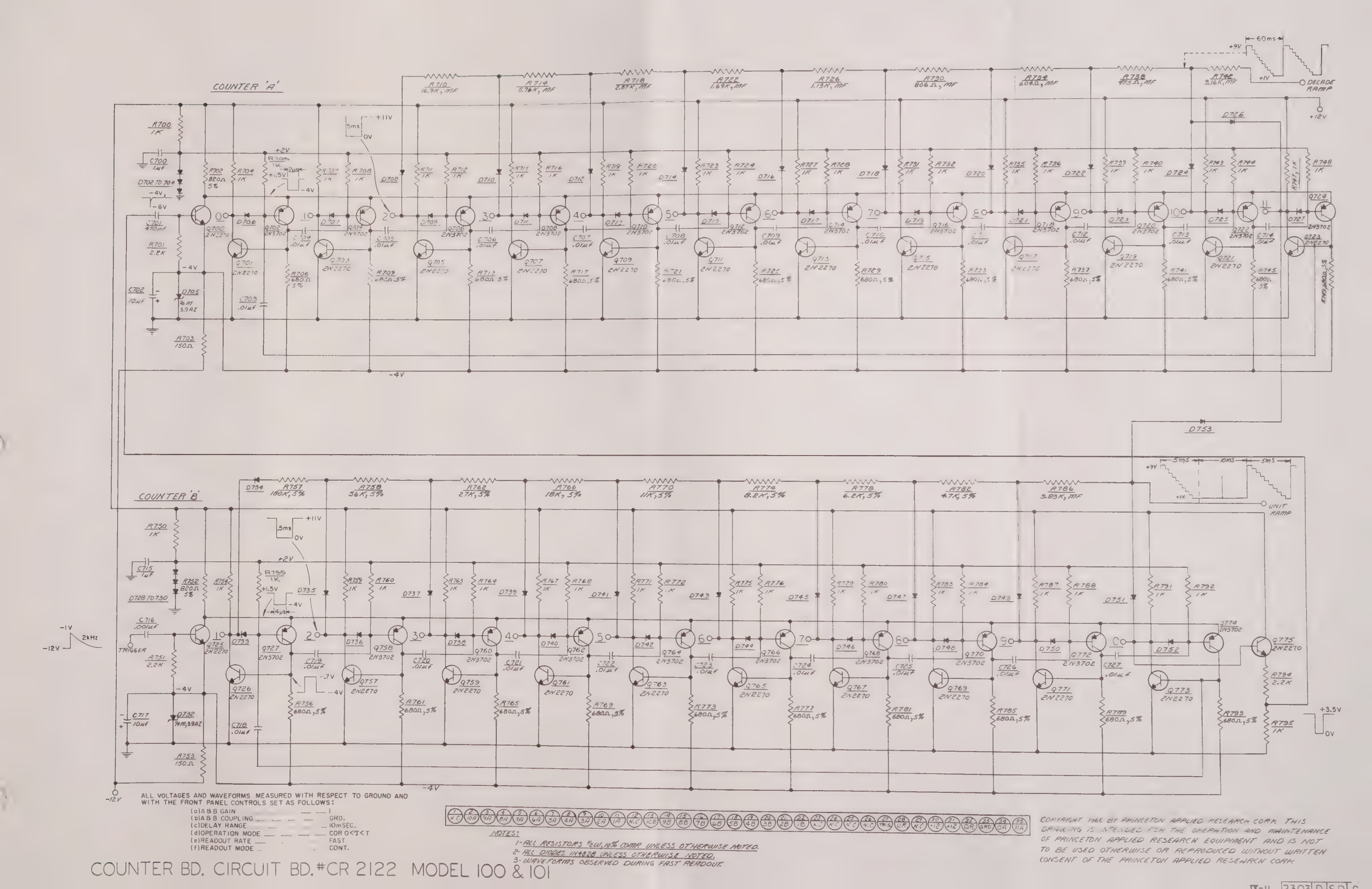
PROGRAMMER BD. CIRCUIT BD.# PR 2125 MODEL 100 & 101

COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORP.

2299 C SD E



COUNTER BOARD LAYOUT DIAGRAM



ALL VOLTAGES AND WAVEFORMS MEASURED WITH RESPECT TO GROUND AND WITH THE FRONT PANEL CONTROLS SET AS FOLLOWS:

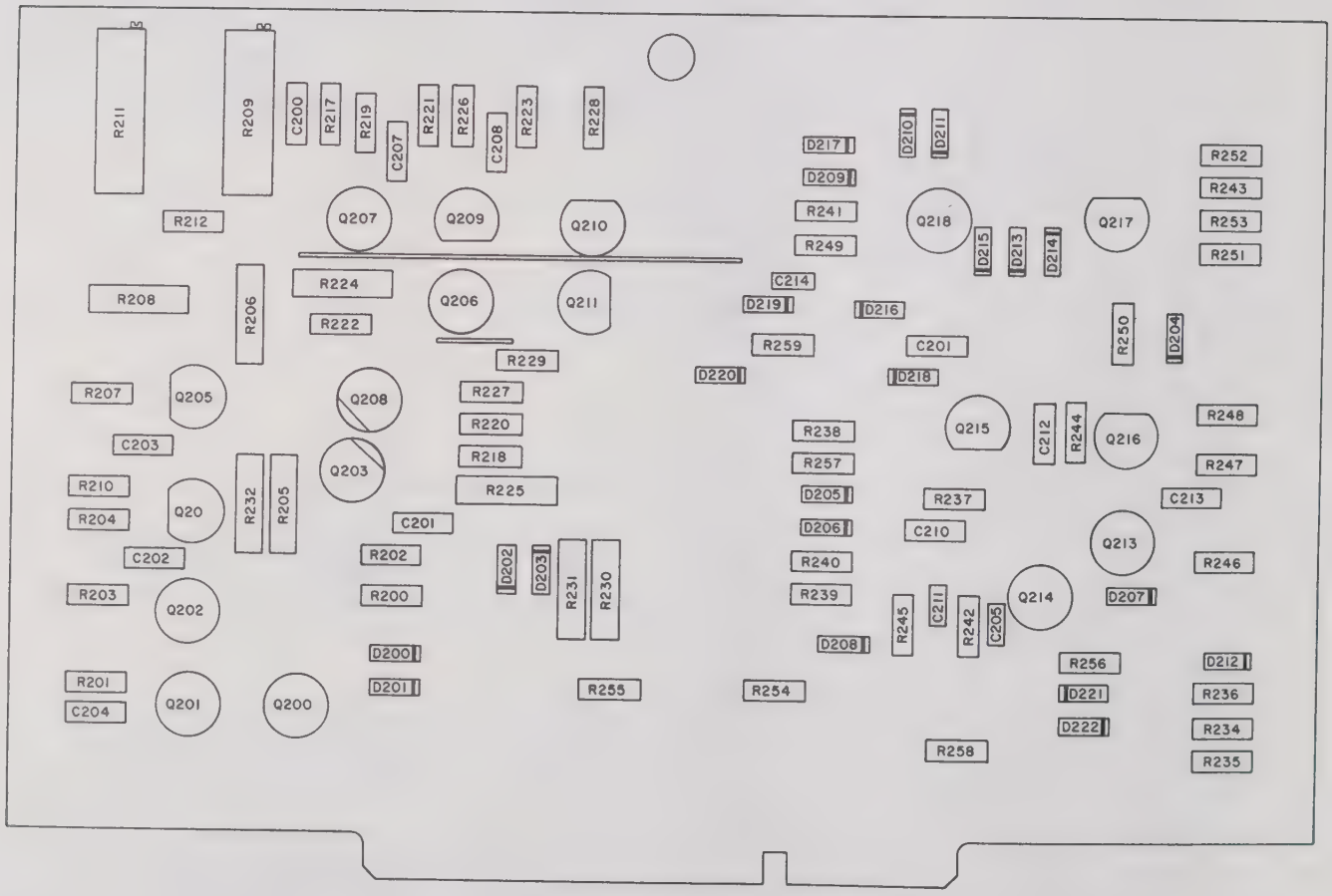
(a) A & B GAIN
(b) A & B COUPLING — GRD.
(c) DELAY RANGE — 10mSEC.
(d) OPERATION MODE — COR 0<T<T
(e) READOUT RATE — FAST
(f) READOUT MODE — CONT.

NOTES:

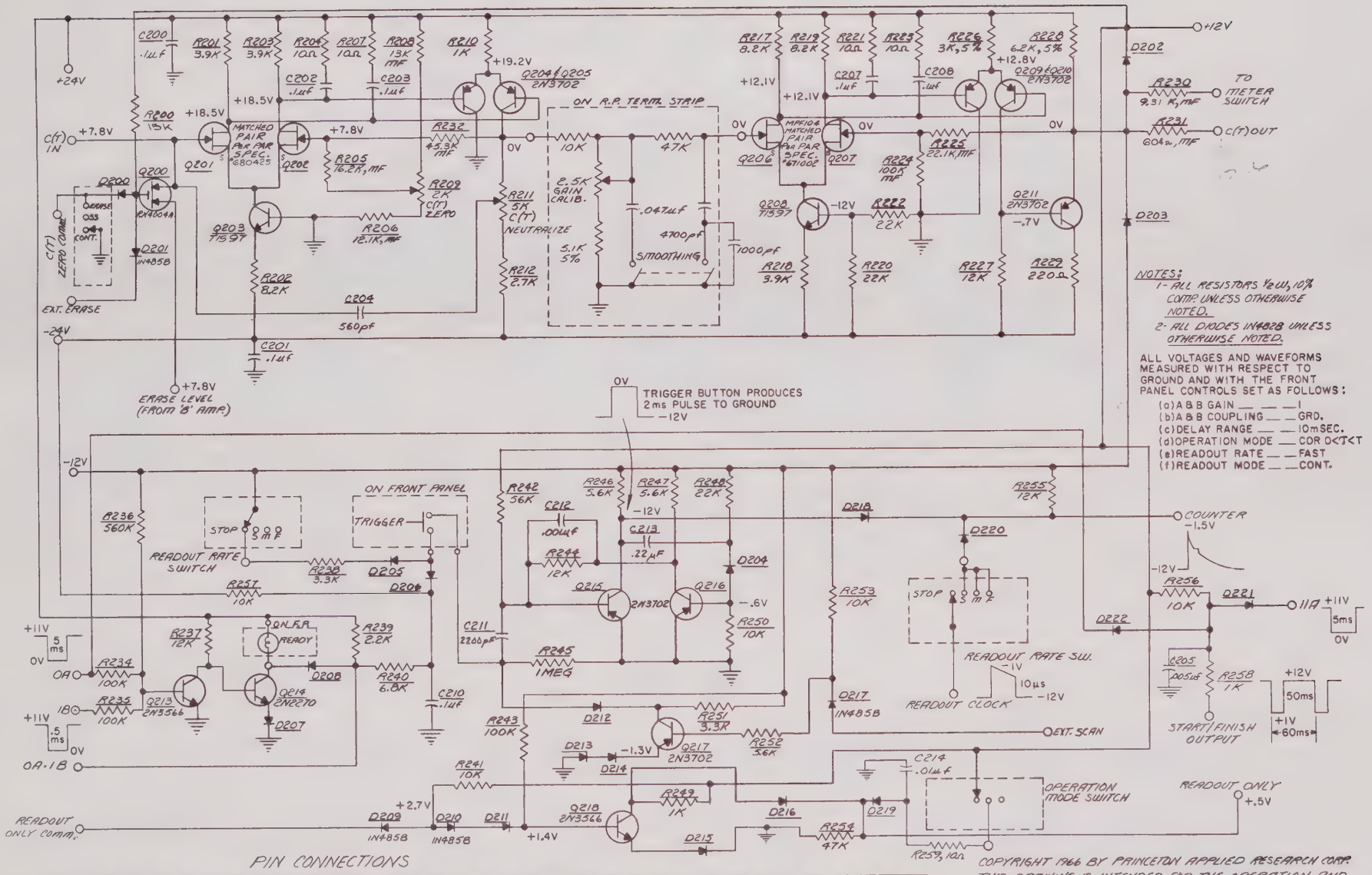
1- ALL RESISTORS ¼W, 10% COMP. UNLESS OTHERWISE NOTED.
2- ALL DIODES IN4828 UNLESS OTHERWISE NOTED.
3- WAVEFORMS OBSERVED DURING FAST READOUT.

COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORP.

COUNTER BD. CIRCUIT BD. #CR 2122 MODEL 100 & 101



OUTPUT BUFFER BOARD LAYOUT DIAGRAM

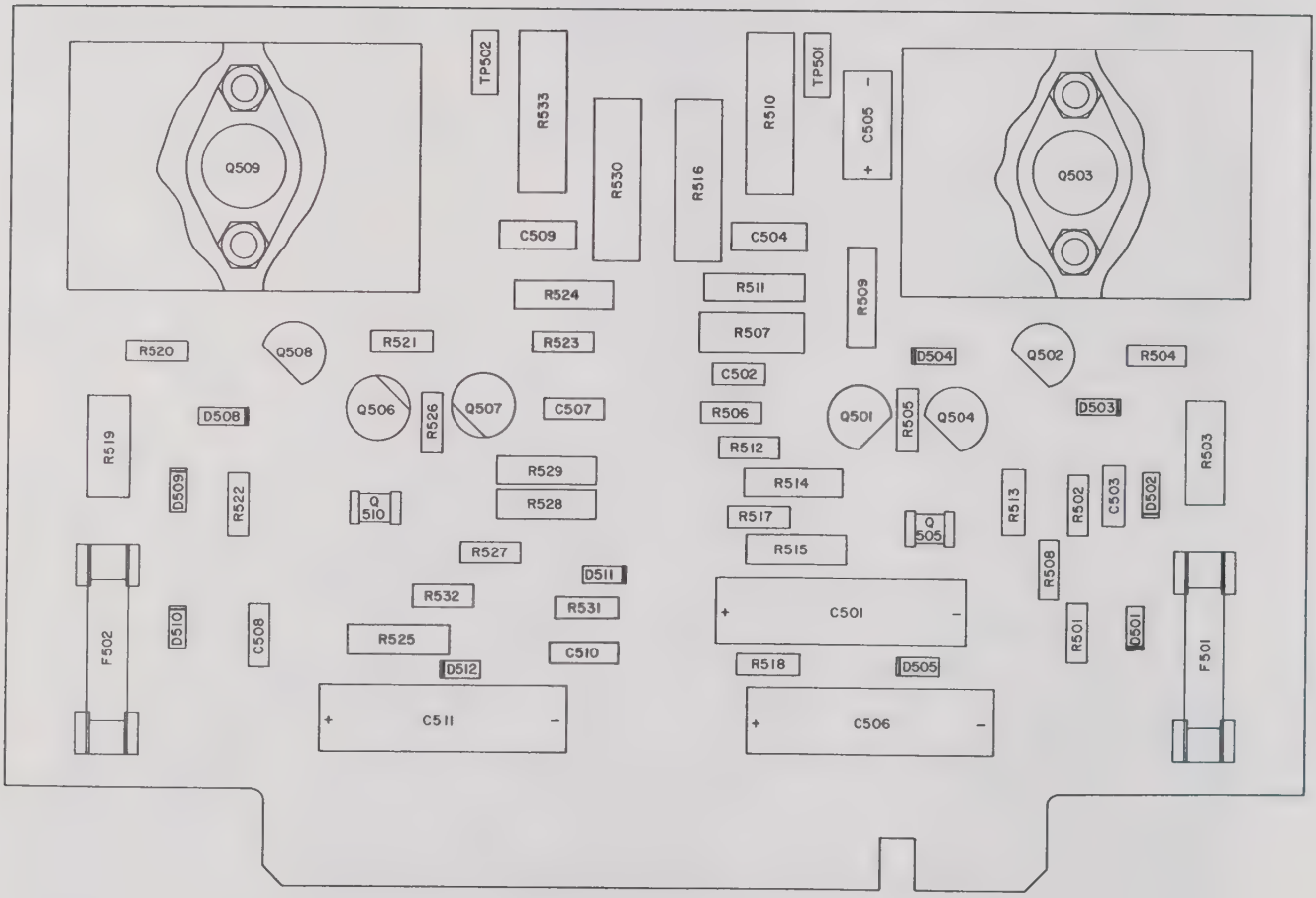


COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORP.

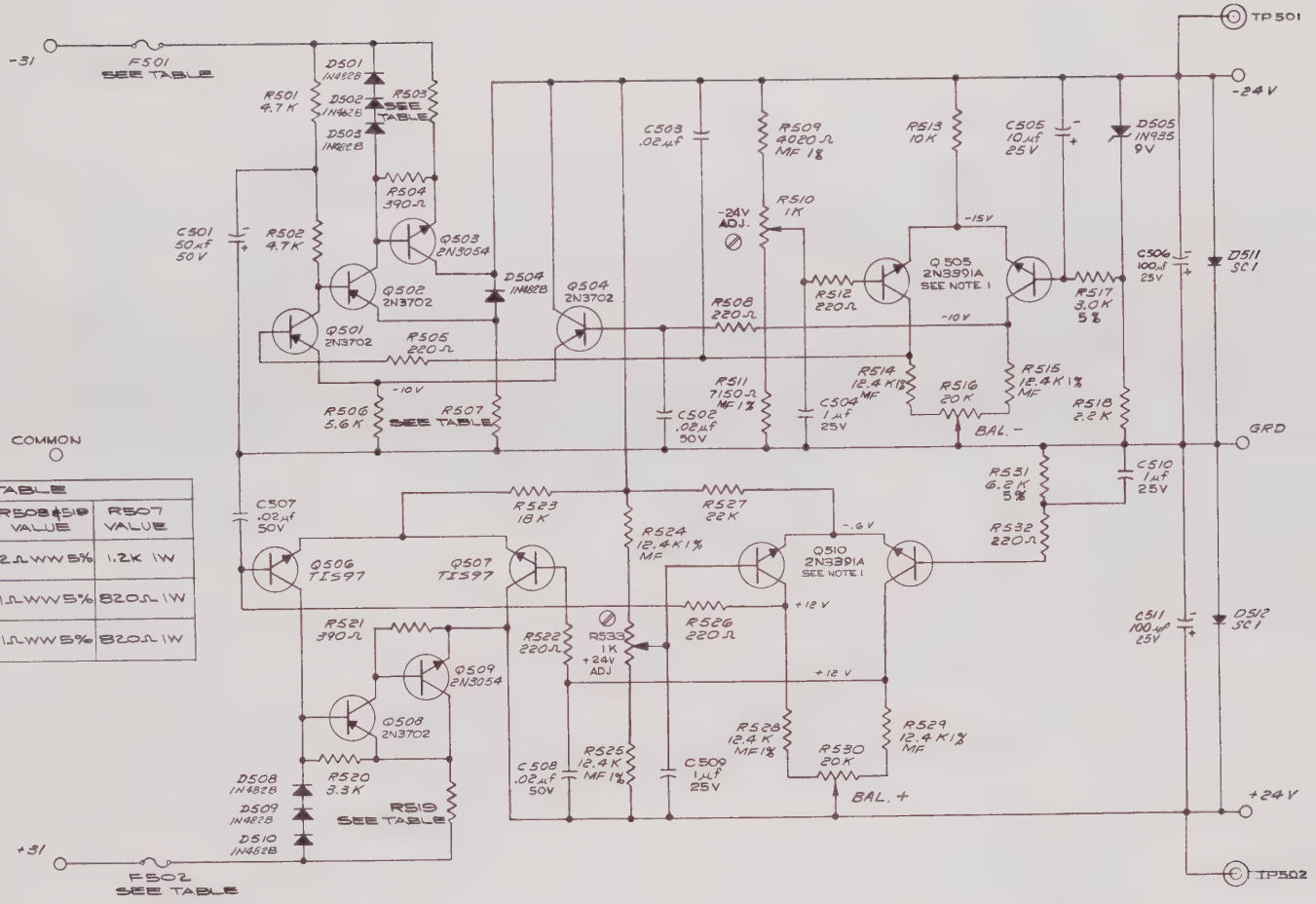
IX-12

OUTPUT BUFFER BD. SCHEMATIC — CIRCUIT BD. #OB2131 — MODEL 100 AND 101

2298 C SD1L



POWER SUPPLIES I & II LAYOUT DIAGRAM



FUSE TABLE			
MODEL	F501 & 502 VALUE	R508 & 519 VALUE	R507 VALUE
HR-8	3AG, 3/8A FAST-BLO	2.2Ω WW 5%	1.2K 1W
TDH-9	3AG, 5/10A FAST-BLO	1.5Ω WW 5%	820Ω 1W
100 & 101	3AG, 5/10A FAST-BLO	1.5Ω WW 5%	820Ω 1W

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
-31	N.C.	N.C.	N.C.	-24	-24	-24	N.C.	N.C.	N.C.	COMMON IN	N.C.	GRD	GRD	GRD	N.C.	N.C.	+24	+24	+24	N.C.	N.C.	+31

CONNECTOR PIN CONNECTIONS

NOTE

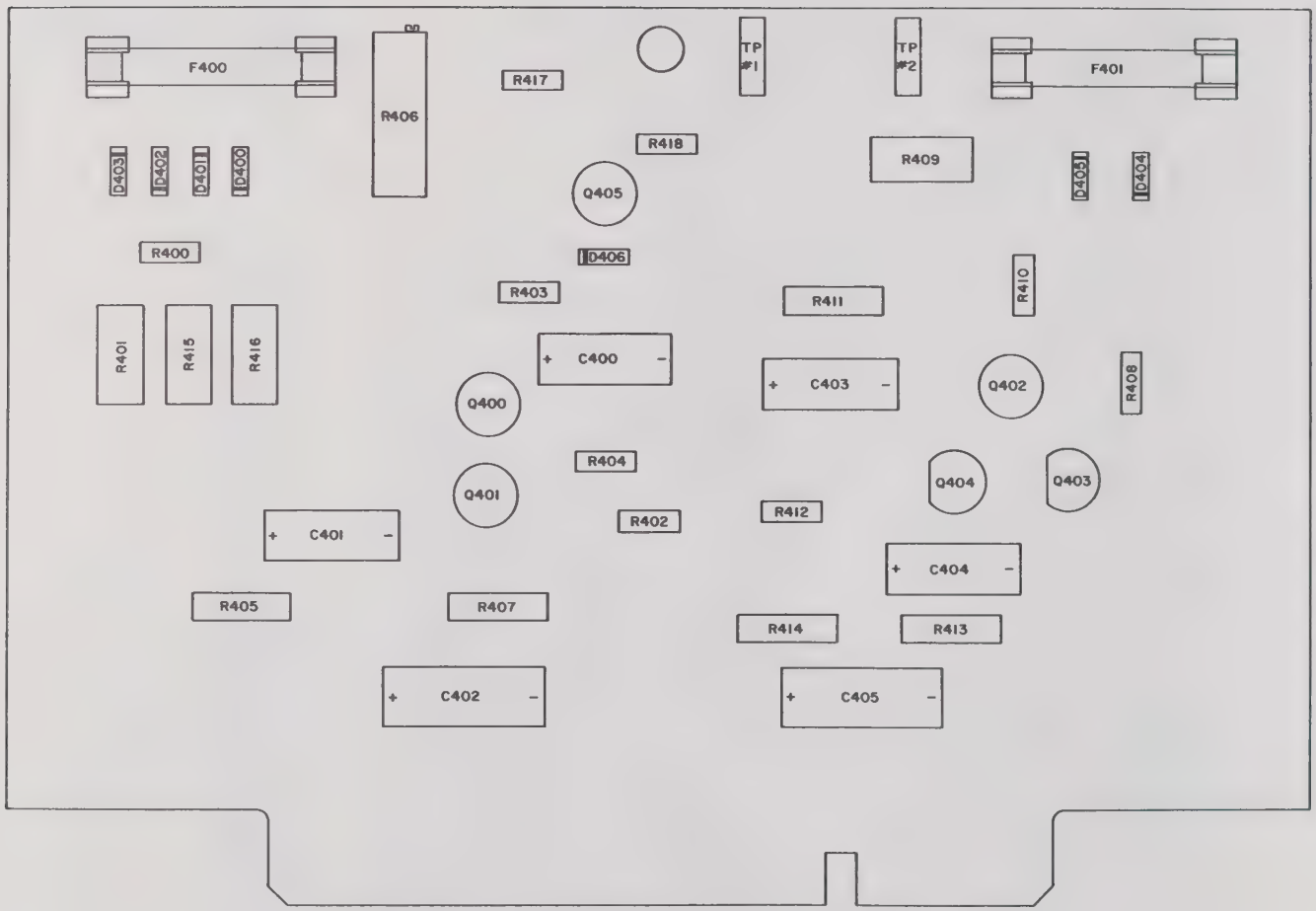
1. Q 505 & Q510 ARE DIFFERENTIAL PAIR E_{BE} MATCHED @ 100μa (SPEC.# 650412 - GREEN)
2. 2N3711 & TIS97 TRANS. MAY BE SUBSTITUTED FOR 2N3391A TRANS.

COPYRIGHT 1965 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORP.

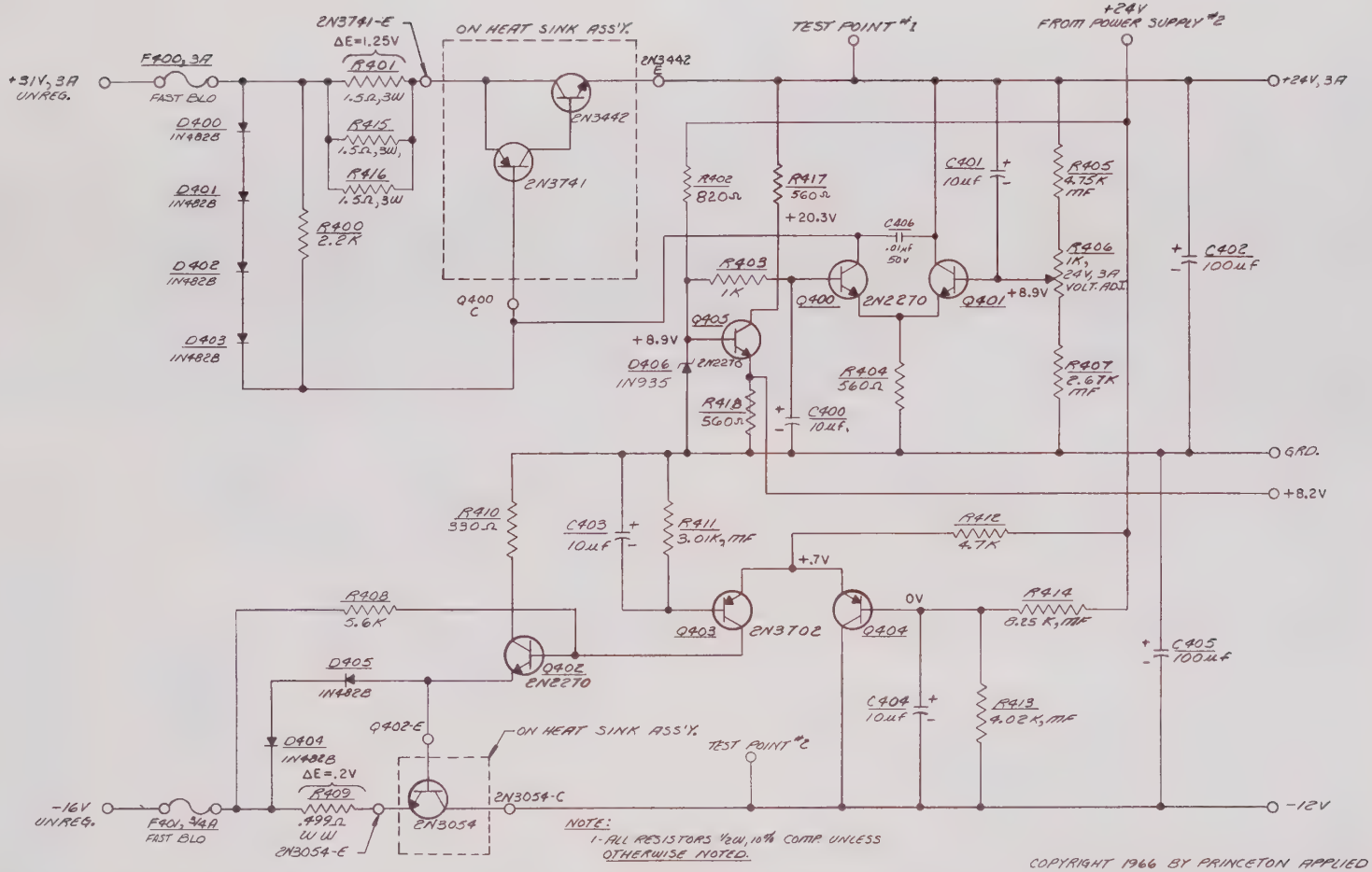
CIRCUIT BOARD Nº. P01396 (HR-8 & TDH-9)
Nº. P0 1800 (SM-1)

POWER SUPPLIES I & II

1387 | C | SD | J



POWER SUPPLY III LAYOUT DIAGRAM

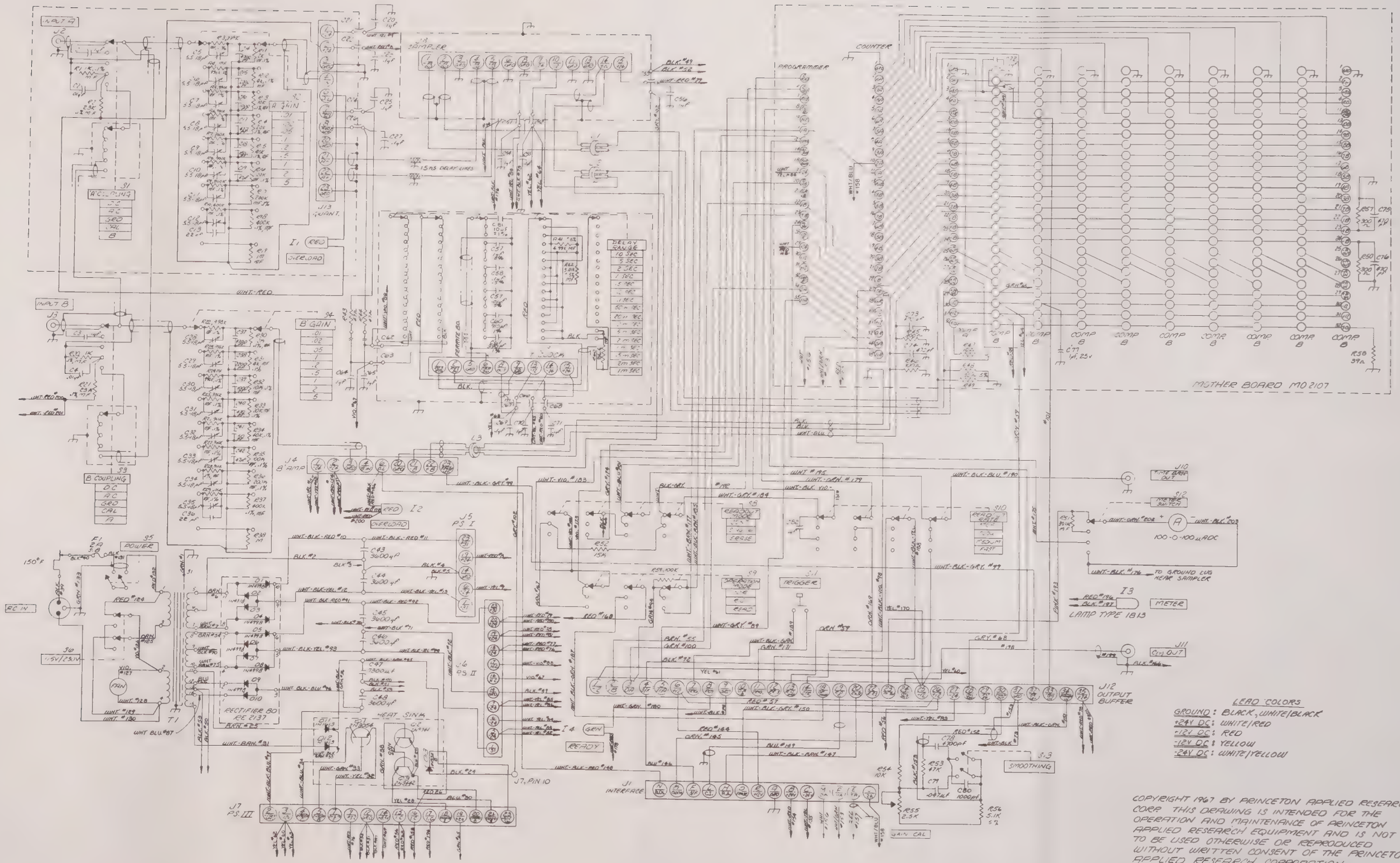


1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
N.C.	-16V UNREG.	-12V	2N3054 C	2N3054 B	N.C.	2N3054 E	N.C.	FROM PS 2 E	N.C.	N.C.	GRD.	N.C.	+8.9V	I.C.	I.C.	I.C.	2N3442 E	+24	2N3741 B	2N3741 E	N.C.	+31V UNREG.

PIN CONNECTIONS

COPYRIGHT 1966 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.

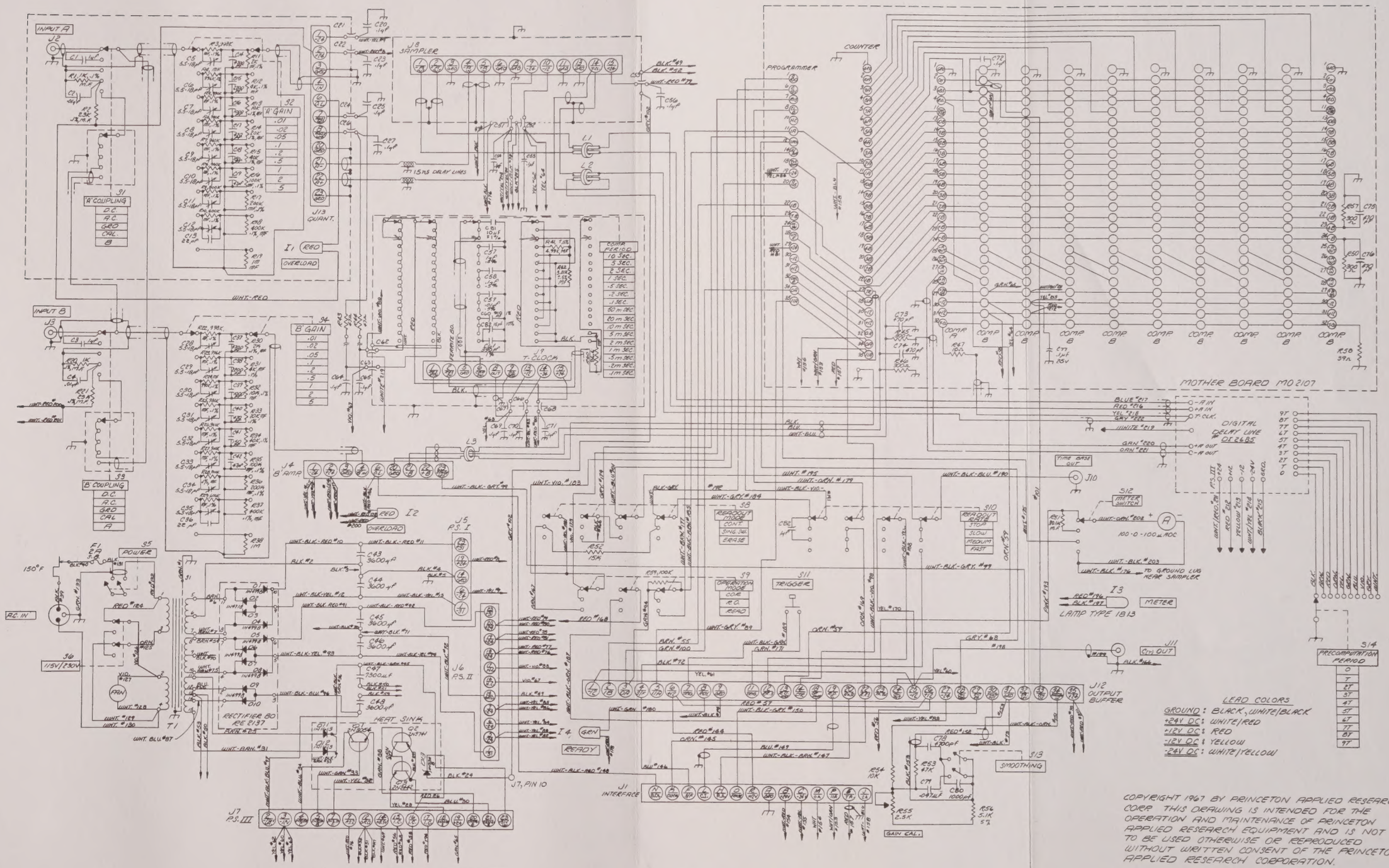
POWER SUPPLY #III SCHEMATIC / MODEL 100 AND 101 / CIRCUIT BD #PS2134



CHASSIS WIRING SCHEMATIC

MODEL 100

COPYRIGHT 1967 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION



CHASSIS WIRING SCHEMATIC

MODEL 101

COPYRIGHT 1967 BY PRINCETON APPLIED RESEARCH CORP. THIS DRAWING IS INTENDED FOR THE OPERATION AND MAINTENANCE OF PRINCETON APPLIED RESEARCH EQUIPMENT AND IS NOT TO BE USED OTHERWISE OR REPRODUCED WITHOUT WRITTEN CONSENT OF THE PRINCETON APPLIED RESEARCH CORPORATION.